Design Study Report

Prepared for:
National Aeronautics and Space Administration
Goddard Space Flight Center
Greenbelt, Maryland

Design Study for Multi-Channel Tape Recorder System

Volume I

AED R-3775F
January 20, 1972
In Response to:
Contract No. NAS5-21511

RCA

RCA|Government and Commercial Systems
Astro-Electronics Division|Princeton, New Jersey

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16. Abstract

The report covers a study of the means of storing multi-spectral, high-resolution sensor data on an Earth-observing satellite. It is concluded that this is best done digitally on a multi-track, longitudinal, magnetic tape recorder. The machine proposed will store 8×10^{10} bits of data on 1040 m of 51-mm-wide magnetic tape mounted on two co-planar reels. A direct-coupled, servo-controlled, brushless, dc torque motor will pull the tape, and a negator spring system or another direct-coupled, dc torque motor will keep the tape at the correct tension. A 112-track, mono-block, hard, read-write, magnetic head will be used. These tracks will carry the digitized data and an overhead of additional bits for synchronization, de-coding, de-skewing, de-jittering, and error correction. The machine will accept as an input a serial bit stream of 40 Mb/s for 30 minutes and play back the data synchronously in 10 minutes as two 65 Mb/s bit streams in phase quadrature for modulating a wideband transmitter. Although data packing densities as high as 0.8 Mb/m will be used, the redundancy built into the system will keep the bit error rate lower than 10^{-8} or allow the loss of a complete data track and still maintain a bit error rate of 10^{-5}. The machine should have a two-year operational life and is expected to occupy 46 liters, weigh 27 kg, and consume 20 W, averaged over one orbit.

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PREFACE

This report describes the primary Multi-Channel Tape Recorder and favored alternate approaches. The studies and tradeoffs that led to the selection of the primary system are also described.

The design work was performed by the Astro-Electronics Division of RCA for the National Aeronautics and Space Administration (NASA), Goddard Space Flight Center (GSFC) under Contract No. NAS5-21511, during the period starting September 4, 1970 and ending May 31, 1971. The work was monitored by Carl Powell, Technical Officer, Flight Data Storage Branch of GSFC. Engineering personnel who contributed to the technical content of this report are listed in Section 6.0.

The system description includes block diagrams; logic diagrams; schematic circuits; outline drawings; sketches; size, weight, and power estimates; and operational descriptions. Link requirements for preserving data quality have been studied. An outline of the ground-station data processing is presented.

It is concluded that the technology required to build a spacecraft tape recorder is available and that the life and reliability requirements can be met by applying the available knowledge of magnetic tapes, magnetic heads, of the recently gained knowledge of the environment in which they operate, and by the selective use of redundancy.

During the study of the matter of storing for 30 minutes analog, high-resolution, multi-channel, spectrometer data on Earth-observing spacecraft, from the sensor outputs to the retrieval of multi-channel analog data of acceptable quality at a ground station, it was concluded that this is best done by first multiplexing the input data and then converting it to a single digital bit stream outside the tape recorder. The data stream should be processed digitally to produce 112 channels, 91 of

which are data, 7 are check bit channels for later error correction in the ground station, and 14 are clock tracks for timing. The 8×10^{10} check and data bits can then be stored on a reel-to-reel coplanar tape transport having 1040 m (3400 ft.) of 50.8-mm (2-in.) wide, 0.03-mm (0.0011-in.) thick magnetic tape, running at 0.577 m/s (22.7 in./s) in record and (for a 3:1 speedup) at 1.73 m/s (68 in./s) in playback.

To minimize pulse crowding, the data should be recorded by high-efficiency, narrow-gap, magnetic heads in delay code and be equalized, filtered, and limited on playback. This will allow 0.8 Mb/m (20 kb/in.) per track of data-packing density. The tape should be moved by a high-efficiency, servo-controlled, brushless, dc motor without belts, gears, clutches, or mechanical brakes. Tape tension may be provided by a Negator-spring system or possibly by another brushless, dc, torque motor. It will be necessary to decode, deskew, and de-jitter the 98 data and check tracks on playback, using the 14 clock tracks. The data may then be re-assembled into a four-phase bit stream, in a form suitable for modulating a wideband transmitter.

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LIST OF ABBREVIATIONS

BCH	Bose - Chaudhuri (Code)
DD	Double-density (code); also referred to as "delay code"
ECAP	Electronic Circuit Analysis Program
EOO	Exclusive-OR Output
NRZ(L)	A NRZ code wherein a change of state ("1" to "0" or "0" to "1") is indicated by a change of level.
PAM	Pulse Amplitude Modulated
PT	Parallel Transfer (Pulse)
PWM	Pulse-Width Modulator
TDM	Time-Division Multiplex
TTL-S	TTL with integrated Schottky barrier diode clamping
VCM	Voltage-controlled multivibrator
VCO	Voltage-controlled oscillator

1.0 INTRODUCTION AND SUMMARY

1.1 Objective

The objective of this report is to describe the primary multi-channel tape recorder system and favored alternate approaches. The studies and trade-offs which lead to the selection of the primary system are also described.

1.2 Scope

The scope of the study is defined in Contract NAS5-21511 entered into on 4 September 1970, and in GSFC Specification S-731-P-99 dated June 1969 for a Wide-Band Multitrack Tape Recorder for Satellite Applications. This design study report is prepared in accordance with the requirements of GSFC Specification S-250-P-1B, March 1970, Amendment 1, 14 November 1970, Contractor-Prepared Monthly, Periodic, and Final Reports.

The system description includes block diagrams, timing diagrams, logic diagrams, schematic circuits, outline drawings, sketches, size, weight and power estimates, and operational descriptions. The reasons are stated herein for selecting a digital rather than an analog system, a co-planar rather than a co-axial tape transport, and a direct brushless dc servo drive rather than a belted synchronous hysteresis drive. Link calculations for the various modes of operation and a block diagram of the ground-station processing equipment are provided, together with a description of its operation. The results of a preliminary study of the input-data multiplexing and analog-to-digital conversion processes are given.

1.3 Conclusion

On the basis of reliability, durability, performance, versatility, growth potential, reasonable size, weight and power consumption, and implementation by the advanced techniques that

will be available when design fulfillment starts, a co-planar tape transport was selected, controlled by a brushless, dc servo having single digital input and four-phase digital output, with a substantial measure of redundancy in processing and data handling. A key feature of the proposed approach is a de-jittering and de-skewing buffer, which allows all time-base error to be removed from the data before transmission. A mix of various, electrically compatible MSI and LSI logic families is proposed to obtain the required speed with minimum power.

1.4 Proposed Data Storage System

The major features of the proposed system are shown in Table 1-1 and Figure 1-1, the block diagram. Figures 1-2 and 1-3 are photographs of experimental model primary and alternate tape transports. Figure 1-4 shows a coaxial tape transport.

The diagram shows the sensors and signal processing equipment producing a serial digital data stream. (After an initial study and discussion with NASA GSFC, this was ruled to be outside the MCTR system, as it will be particular to each spacecraft sensor complement).

The serial NRZ data will first be converted into 91, parallel, bit streams by serial-parallel de-multiplexing logic. From the 91 data bits, 7 check bits will be generated by the Bose-Chaudhuri method. The input clock will also be processed to produce 14 separate clock and synchronization streams.

The Bose-Chaudhuri (BCH) encoder will be the 127, 120, 1) type; that is, there will be 127 bits per word, of which 120 will be data bits and 7 check bits. This will permit one error per word to be corrected or two errors to be detected. For the MCTR, only 91 data bits are required per word. These 91 bits plus the 7 check bits will comprise the 98-bit data word, each

TABLE 1-1. MULTI-CHANNEL TAPE RECORDER FEATURES

CHARACTERISTIC	VALUE
Capacity	8×10^{10} bits
Density	0.8 Mb/m (20 kb/in.) Delay Code
Number of Tracks	91 data +7 check +14 clock
Times	30 min. write, 10 min. read (fast), 30 min. read (slow)
Speeds	0.577 m/s (22.7 in./s) write, 1.73 m/s, (68 in./s) read (fast) 0.577 m/s (22.7 in./s) read (slow)
Tape	3M 551, 1040 m (3400 ft) long 50.8 mm (2 in.) wide, 0.03 mm (0.00113 in.) thick, including 5 µm (0.00021) in.) coating.
Heads	1 erase; 1 write-reat Track spacing 0.5 mm (0.02 in.) Track width 0.3 mm (0.012 in.), gap 0.9 µm (35 µ in.), tape-head separation 0.5 µm (20 µ in.).
Size	Transport: 550 mm (21.5 in.) x 364 mm (14.3 in.) x 210 mm (8.25 in.), Electronics: 127 mm (5 in.) x 200 mm (8 in.) x 152 mm (6 in.).
Weight	Transport: 23.2 kg (51 lb) Electronics: 4.1 kg (9 lb)
Power	29W write, 107W read (fast), 103W read (slow).

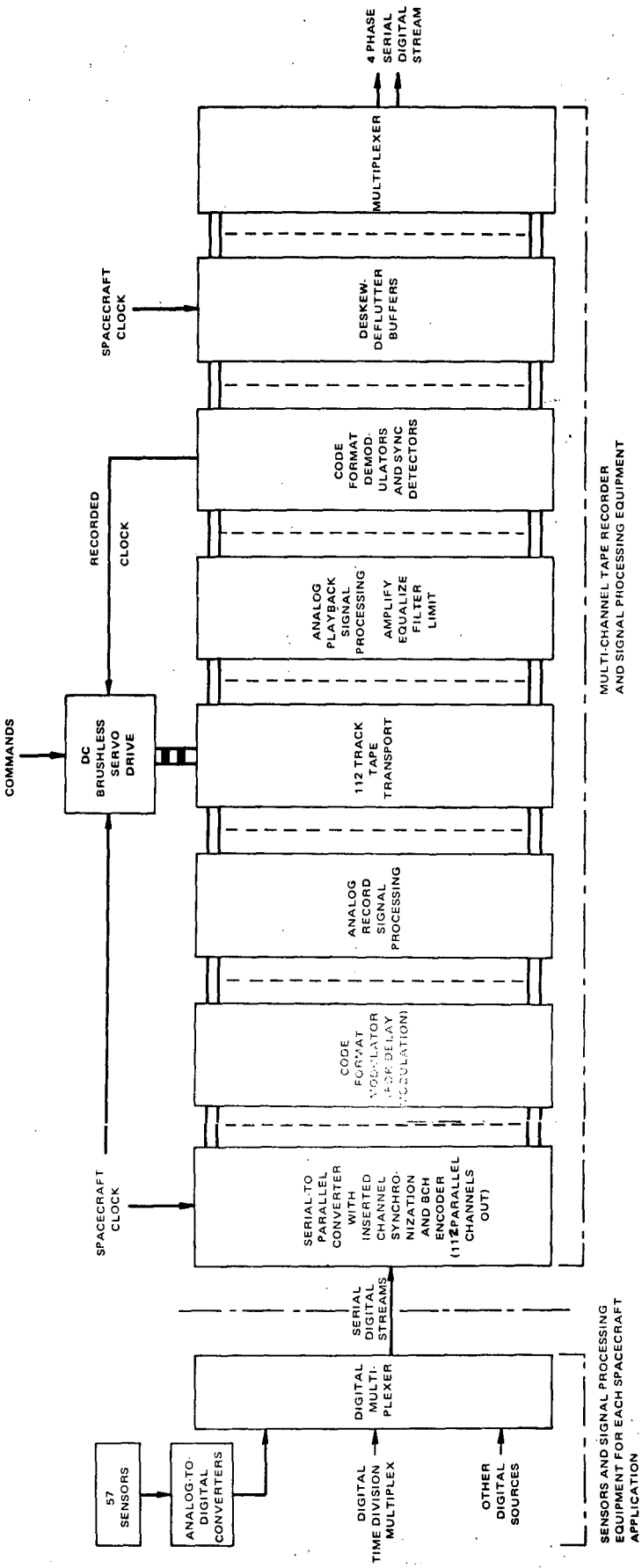

Figure 1-1. Multi-Channel Tape Recorder System, Functional Block Diagram

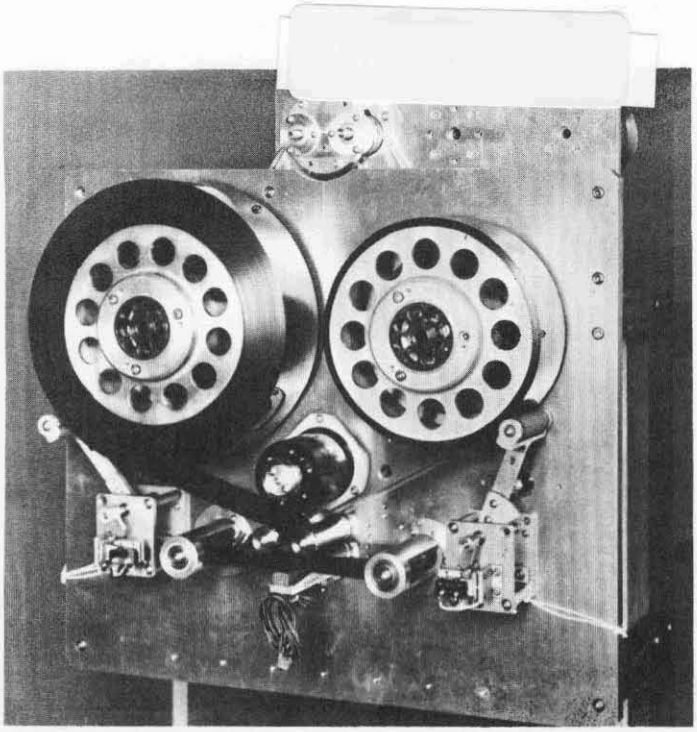

Figure 1-2. Experimental Model (Primary) Tape Transport

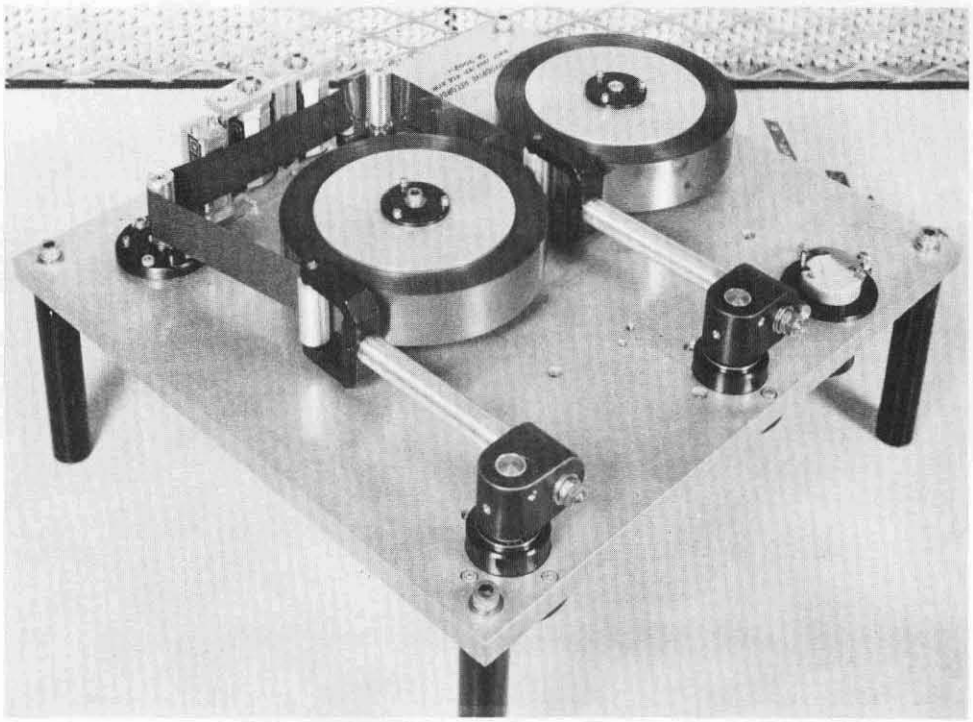

Figure 1-3. Experimental Model (Alternate) Tape Transport

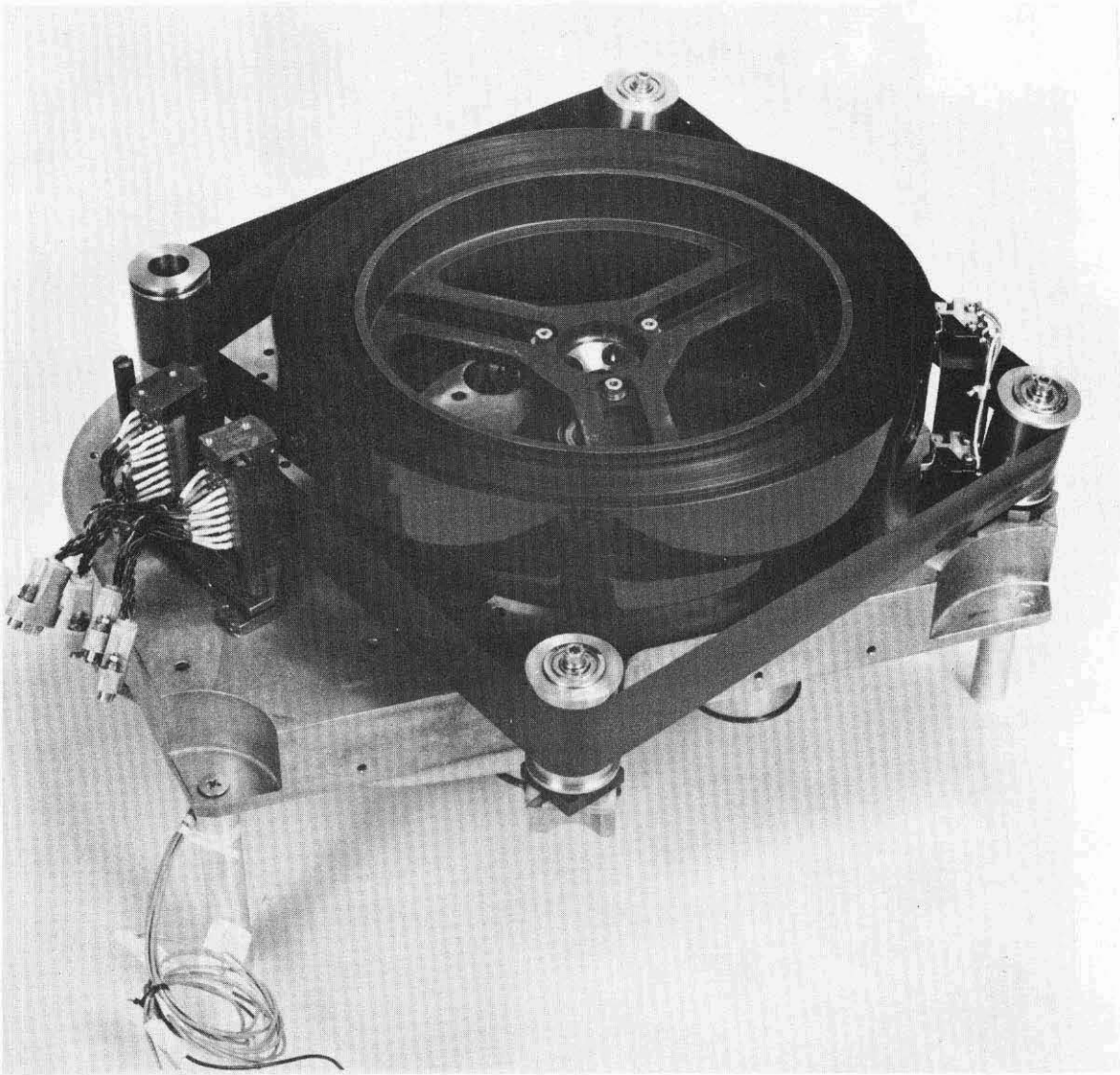

Figure 1-4. Coaxial Tape Transport

bit of which will be recorded on a separate tape track. This format still has the single-error-correction, double-error-detection features of a fully employed BCH code.

The de-multiplexing logic will consist of three stages of serial-to-parallel conversion, in order to be compatible with the BCH encoder timing and to maximize the portion of circuitry performing low-speed (and hence low-power) switching. The de-multiplexing switches will be in the sequence 1:7, 1:2, 1:7, providing in total 1:98 demultiplexing.

There will be one double-density encoder for each of the 98 tracks. Double-density delay code has a spectral density ideally suited to tape recording.

Separate clock channels will be recorded, despite the self-synchronizing features of delay code, for reasons which follow. Each clock channel will be recorded redundantly to provide ability to survive the loss of a clock track. There will be 7 redundant clock channels and hence, 14 clock tracks. The clock pairs will be located on tracks 8, 9; 24, 25; 40, 41; 56, 57; 72, 73; 88, 89; and 104, 105. The clock signal will be an alternating 1 and 0 sequence that contains a bit complement every 32 bits. These will be recorded synchronously across the full tape width, providing phasing, skew, and decoding timing for the playback signal processing. The 14 clock tracks, together with the 7 check tracks and 91 data tracks, will constitute the 112 tracks of the MCTR.

Code format modulators will convert the 98 NRZ coded tracks to delay code. There will be 112 record amplifiers transforming the logic levels to record currents, which will saturate the previously erased magnetic tape.

A 112-track read-write head is proposed. This will be constructed from four monolithic blocks of hard magnetic head

material. Alfecon II and the ferrites are candidate materials. The head will have a 0.9-μm gap and each track will be 0.3 mm wide. Single turns will couple each track to small ferrite toroidal transformers having multiple secondary turns.

On playback, which will be in the same tape direction as record, the signals from each track will be amplified and equalized in phase and amplitude to restore the zero crossings to their correct locations. To improve the signal-to-noise ratio, the equalizers will be followed by linear phase filters and, to secure immunity from all but the most severe and rarest dropouts, each track will be processed by a low-threshold, zero-crossing detector or hard limiter.

Code format demodulators will convert each of the 98 tracks from delay code back to NRZ. Phase-locked loops on each of the seven clock channels and slack re-phasing logic will provide the clock signals for this conversion. The measured skew on experimental model tape transports indicates the practicability of this approach, which will avoid deriving 98 clocks from the data and will eliminate a great deal of clock-processing hardware.

An eight-bit buffer will be used on each data and check track to remove the skew and jitter. In the buffer, each of the data and check-track outputs will be resynchronized to the stable spacecraft clock. The minimum buffer size is dependent on the total timing error, due to jitter and skew.

The output multiplexer will be a serial-to-parallel converter, consisting of two parallel-in, serial-out shift registers. One register will lag the other by one-half bit to provide the phasing required by the four-phase PM transmitter. The resulting output data will therefore be two serial bit streams, each at 49 times the rate of the clock channels.

The reference signal for the drive servo in playback will be derived from the center clock tracks, 56 and 57. The two tracks will, via an OR gate and divider, produce a frequency that will be compared with the stable spacecraft clock in a frequency and phase detector whose output will be the error signal for the drive servo. A brushless dc drive motor will pull the tape at such a speed as to lock the two clock signals in phase. This system will ensure that the output data are synchronous in both short and long term.

In the primary tape transport proposed, tape tension will be provided by a geared and belted spring negator system, similar to that now in use on the ERTS video tape recorder. Alternately, another dc brushless torque motor will be used to keep the tape in tension while it is in motion. In standby, a brake would lock the tape.

The magnetic tape will be selected, tested, and treated in accordance with the recommendations of the final report of Magnetic Head/Tape Interface Study for Satellite Tape Recorders by the Illinois Institute of Technology Research Institute (Contract NAS5-11622). Magnetic Head materials and wrap angles will also be in accordance with this report. The atmospheric environmental conditions will be controlled by the findings of this study and the AED IR&D program on Tape Recorder Tribology.

Small bearings and bearings running at relatively high sppeds or high loads will be avoided, and the number of rotating parts will be minimized. Based upon the excellent results of life tests and operational use on the Nimbus-HDRSS and TIROS program, the tracking ESSO Andok-C grease is proposed as the lubricant for all bearings.

2.0 DESCRIPTION OF RECOMMENDED SYSTEM

2.1 Digital Signal Processing

2.1.1 Recommended System

The spacecraft system starts with sensor outputs and ends with the down-link transmitter. Sensor outputs are assumed to be the following:

54 channels, each having a 0-to-40-kHz analog baseband
3 channels each having a 0-to-13-kHz analog baseband

The 57 sensor channels are sampled and converted to a serial pulse amplitude modulated (PAM) stream. This time division multiplex (TDM) signal is converted to a seven-bit PCM serial stream with a single A-D converter. The TDM-A unit is tailored to the particular sensors specified for each mission.

The PCM signal (39.9 Mb/s in this case) is encoded with extra bits into a Bose-Chaudhuri, error-correcting code (BCH code). The resulting signal at 43 Mb/s is either sent to the storage tape recorder system or is transmitted to ground in real time, as desired.

The storage system is composed of the record function and later playback at higher speed. The capacity of 8×10^{10} bits permits 30 minutes of recording on 1040m (3400 ft) of tape at 0.577 m/s (22.6 in./s). Playback time is 10 minutes at 1.73 m/s (68 in./s). The output information rate of 129.16 Mb/s is transmitted to ground with a four-phase PM transmitter operating at a keying rate of 64.58 million bauds. Link specifications are given in Section 2.5.

The high storage capacity is achieved by converting the serial input to 98 parallel data channels, each at 438 kb/s. Since the playback output must be in serial form, a parallel-to-serial converter is required. To accomplish this function, it is first necessary to buffer out all time-base error, skew, and jitter.

This results in a perfectly regenerated signal on the down link, completely free of time-base error. In addition to the 98 data tracks, seven sets of parallel sync tracks are dispersed throughout the data tracks. The sync tracks are used for the skew removal. It will be a function of the ground terminal to recover the BCH encoded data, provide error correction capability, and demultiplex the sensor data.

In the overall system, it is a requirement that one master clock provide all of the required timing signals, including the servo clock to control playback tape speed.

The data is double-density (DD) encoded prior to recording the data.

DD encoding is also referred to as delay code, or double density (DD code). This code has half the transition density of biphase code and permits achieving a tape packing density of 0.8 Mb/m (20 kb/in.). This is the same packing density as 0.4 Mb/m (10 kb/in.) with biphase code. DD encoding gives a binary signal with three symbol durations of either one bit, one-and-one-half bits, or two bits. A DD encoder is simply a flip flop that is toggled with a signal composed of the NRZ data logically ORed with the NRZ clock.

The middle data tracks, numbers 55 and 58, are used for servo control of tape speed. Data is recorded at 438 kb/s at a tape speed of 0.577 m/s (22.6 in./s), giving a packing density of 0.8 Mb/m (20 kb/in.). Length of tape to record for 30 minutes is:

$$0.577 \times 30 \times 60 = 1040 \text{ m (3400 ft) of tape.}$$

2.1.2 Record Electronics

The record logic circuitry, shown in the block diagram of Figure 2-1, provides the circuitry for translating the 39.9-Mb/s serial input data into 98 parallel 0.438-Mb/s data channels for channels for recording on the MCTR. The circuitry includes a BCH* data encoder for providing error correction and detection in the data stream, and also generates the timing signals for the recorder clock tracks. The logic also translates the data from NRZ(L) to double density encoded data, for compatibility with the requirements of recording digital data on magnetic tape. The input-signal requirements of the record logic circuitry are only the 39.9-Mb/s serial NRZ(L) data stream and a synchronized 39.9 MHz, square-wave, clock input. The record logic outputs are the 98 data channels, and 14 sync channels.

Serial input data at 39.9 Mb/s is the first BCH encoded by adding seven check bits following each 91 data bits. This is accomplished by buffering the input data and reading out of the buffer at 14/13 times the input rate, leaving a seven-bit gap into which the seven extra bits are inserted. The input-output switch is shown on the diagram to permit bypassing the BCH encoder if desired. This would lower the bit rate and the required switching clock rates in the following circuitry. (Since the seven check bits permit correction of all non-overlapping tape dropouts, or for loss of one parallel channel, it appears that the BCH encoder should always be included.)

The BCH code used is designated as (BCH 127-120-1) which means 127 bit words, 120 information bits, and single error correction. Since there are only 98 channels rather than the full 127, the code word used is equivalent to 29 zeros +91 data bits +7 check bits; the 29 zeros are not transmitted. At the start of the first data bit out of the buffer, the seven-bit shift register is set to the condition it would be in after 29 zeros input to the exclusive -OR circuit. The bit rate out of the BCH encoder is 43 Mb/s.

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*Bose-Chaudhuri

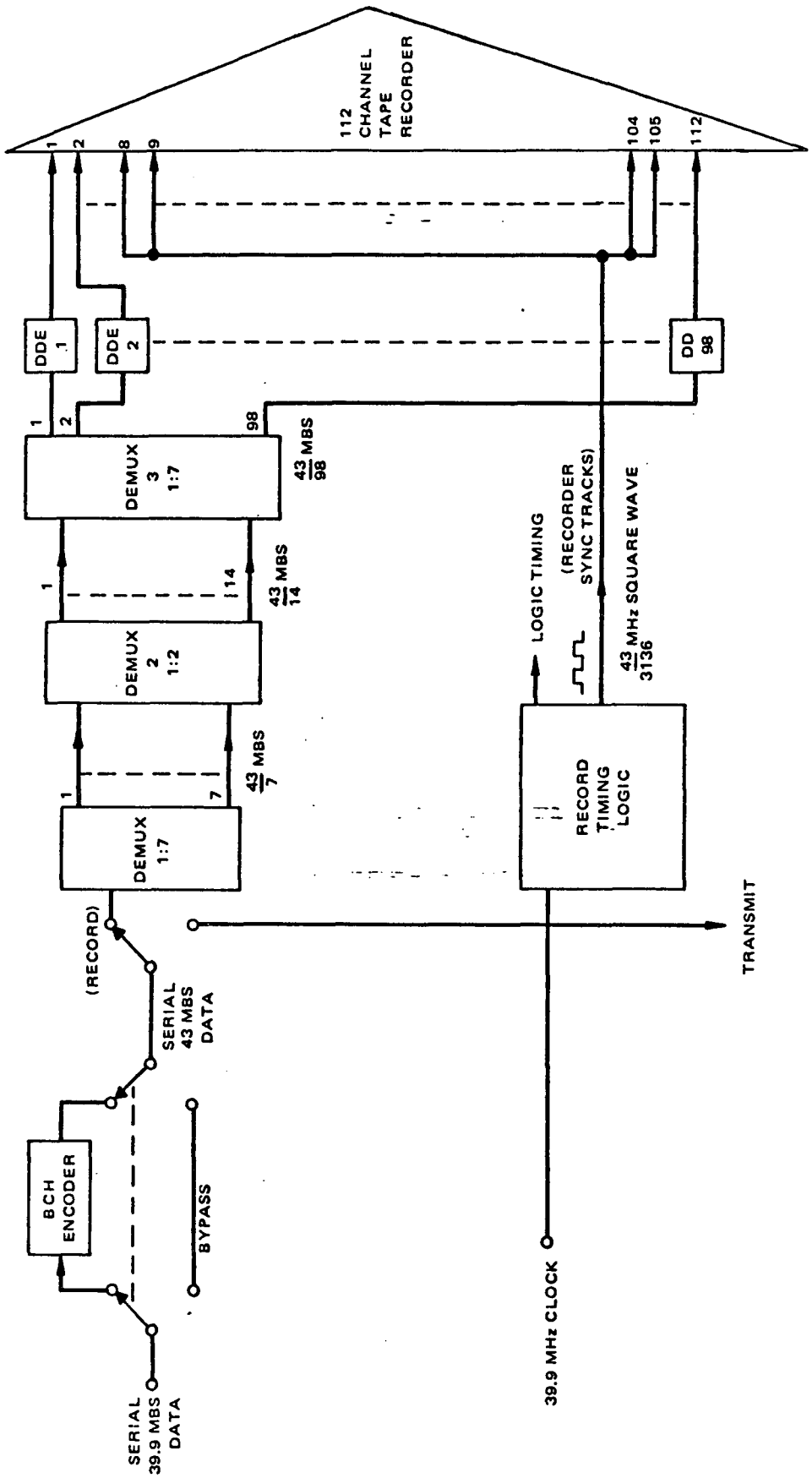


Figure 2-1. Record Electronics, Block Diagram

A block diagram of the BCH encoder is shown in Figure 2-2. The encoder consists of two shift registers, BCH_A and BCH_B. A data frame consists of 91 input data bits and seven additional bits derived from the BCH encoder for error correction. The output rate from the encode circuit is therefore $\frac{91+7}{91}$ (39.9) Mb/s or 43 Mb/s, which corresponds to a data rate increase of 14/13 or 8 percent. The first 91 bits of the output frame are read out of buffer BCH_A while the last 7 bits are derived from BCH_B. The operation of buffer BCH_A can be visualized as follows: Buffer BCH_A is an eight-bit register with simultaneous readin-readout capability. During the time that the error location code is being read out of BCH_B buffer BCH_A is loaded with seven input data bits.

Since the readout rate is 14/13 of the input rate, the number of bits stored in the buffer decreases by one for each 14 bits read out of the register. When a total of 91 bits has been read out, the number of bits remaining in BCH_A will be reduced to zero. The next seven output bits form the error location polynomial and are derived from BCH_B. During this time BCH_A accepts seven input data bits with no readout taking place. The result is that when the frame is complete at bit 98, BCH_A is again loaded with seven input data bits.

The BCH encoder timing chart of Figure 2-3 shows the relative phase between the input and the output of BCH_A during a complete frame. The implementation of BCH_A is shown in Figure 2-4. The buffer, BCH_A, consists of eight storage flip-flops, together with circuitry for clocking the data into and gating the data out of the buffer at the two different data rates. The logic circuitry for developing the input and output clocking circuitry is shown in Figure 2-5. In order to implement the 14/13 clocking ratio, the output is clocked at the same rate as the input for 12 input bits and at twice the input rate during the 13th input bit. The result is that output bits 13, 14, 27, 28, 41, 42,

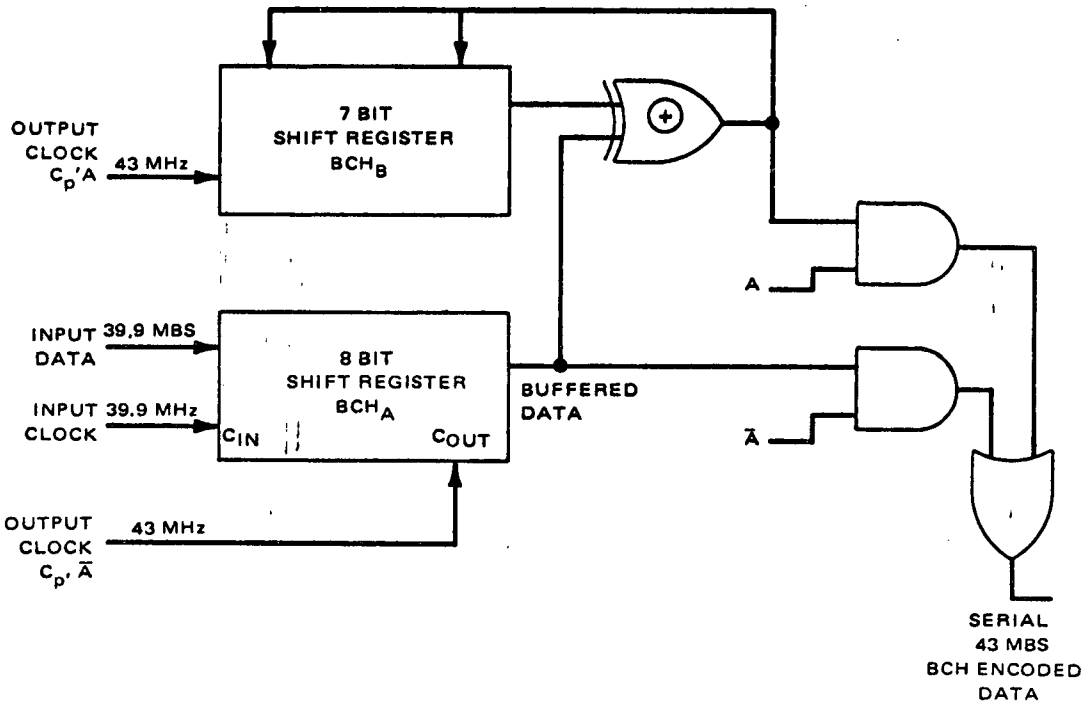


Figure 2-2. BCH Encoder, Block Diagram

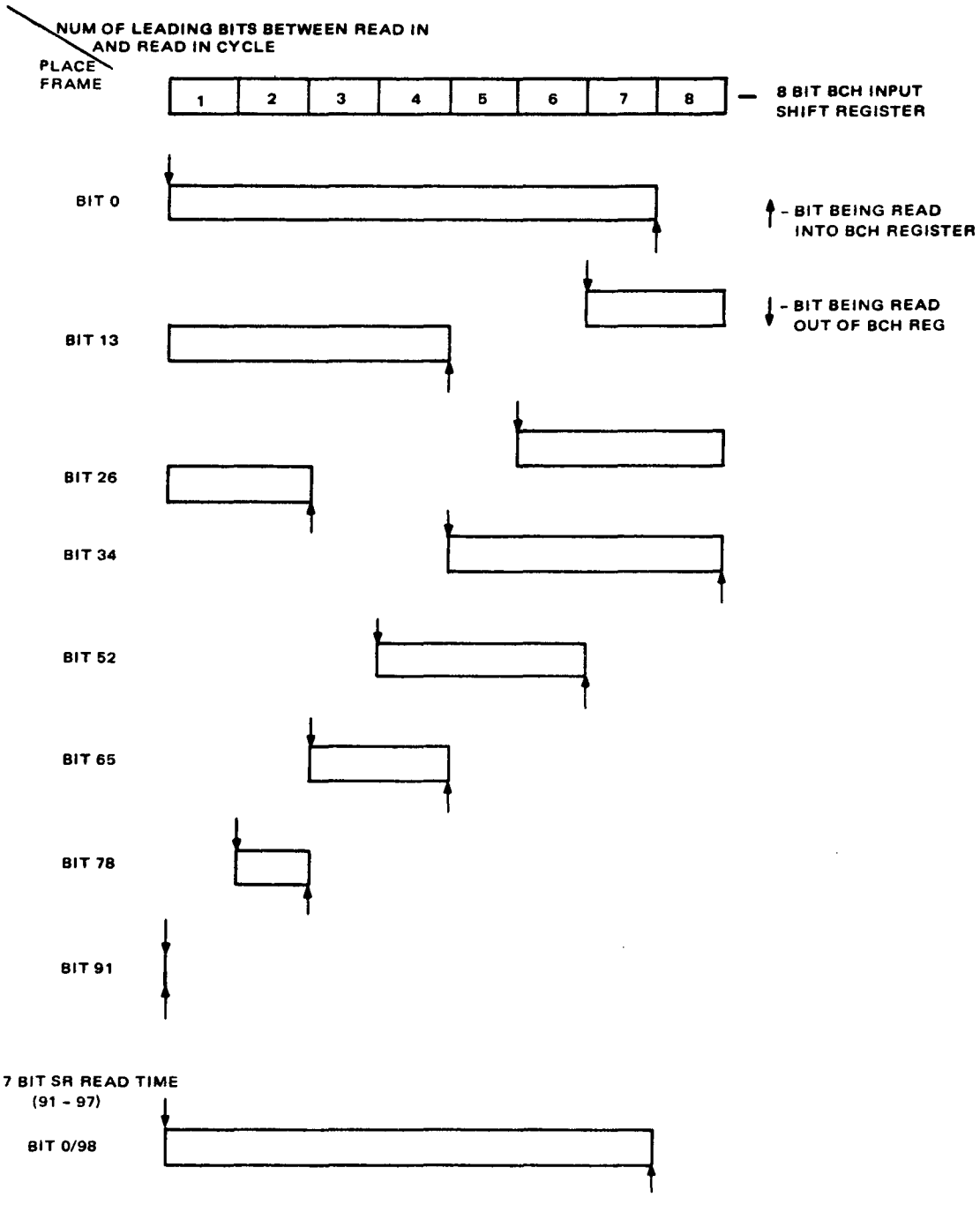


Figure 2-3. BCH Encoder Timing Chart

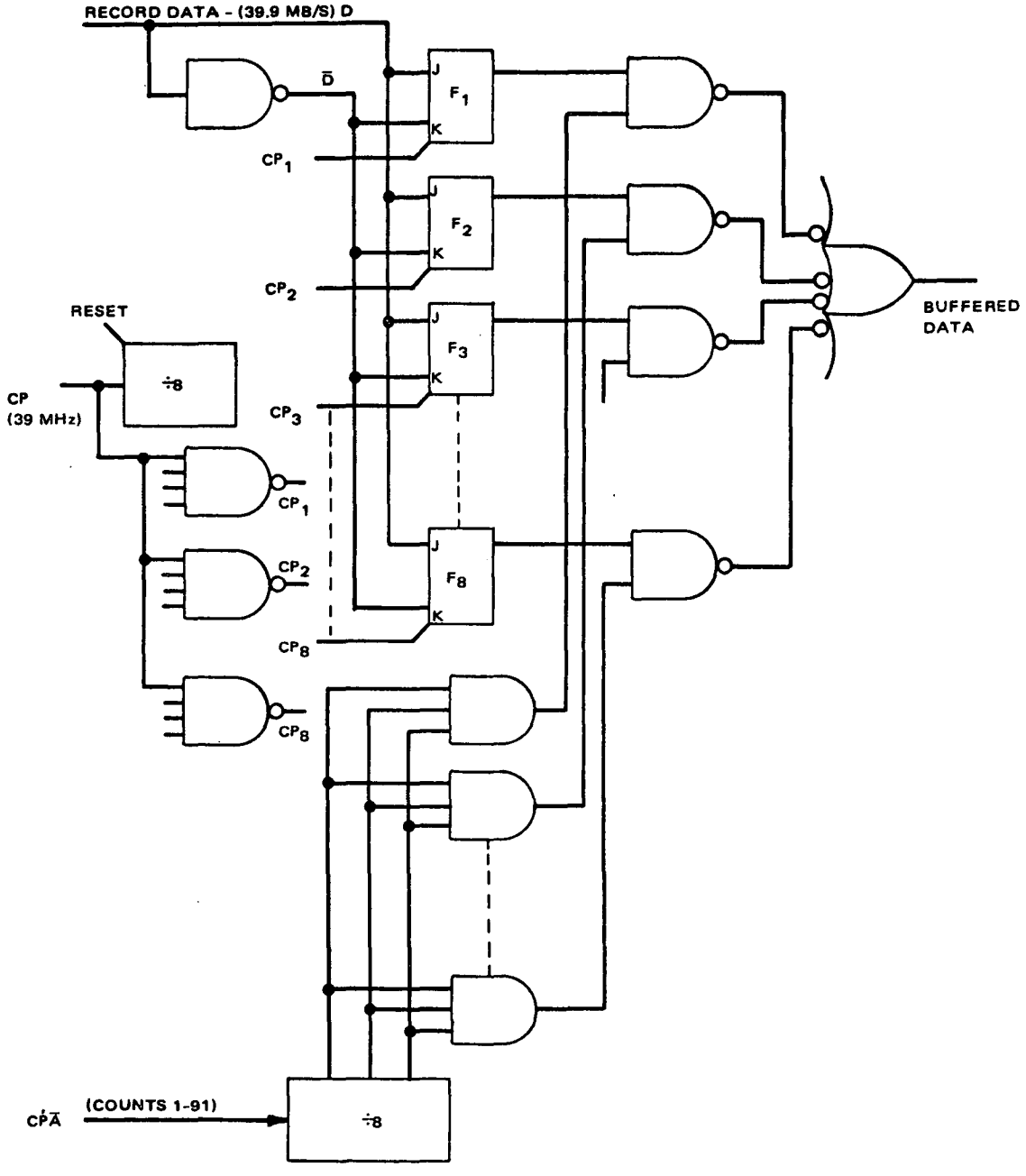


Figure 2-4. Detail of Eight-Bit Buffer

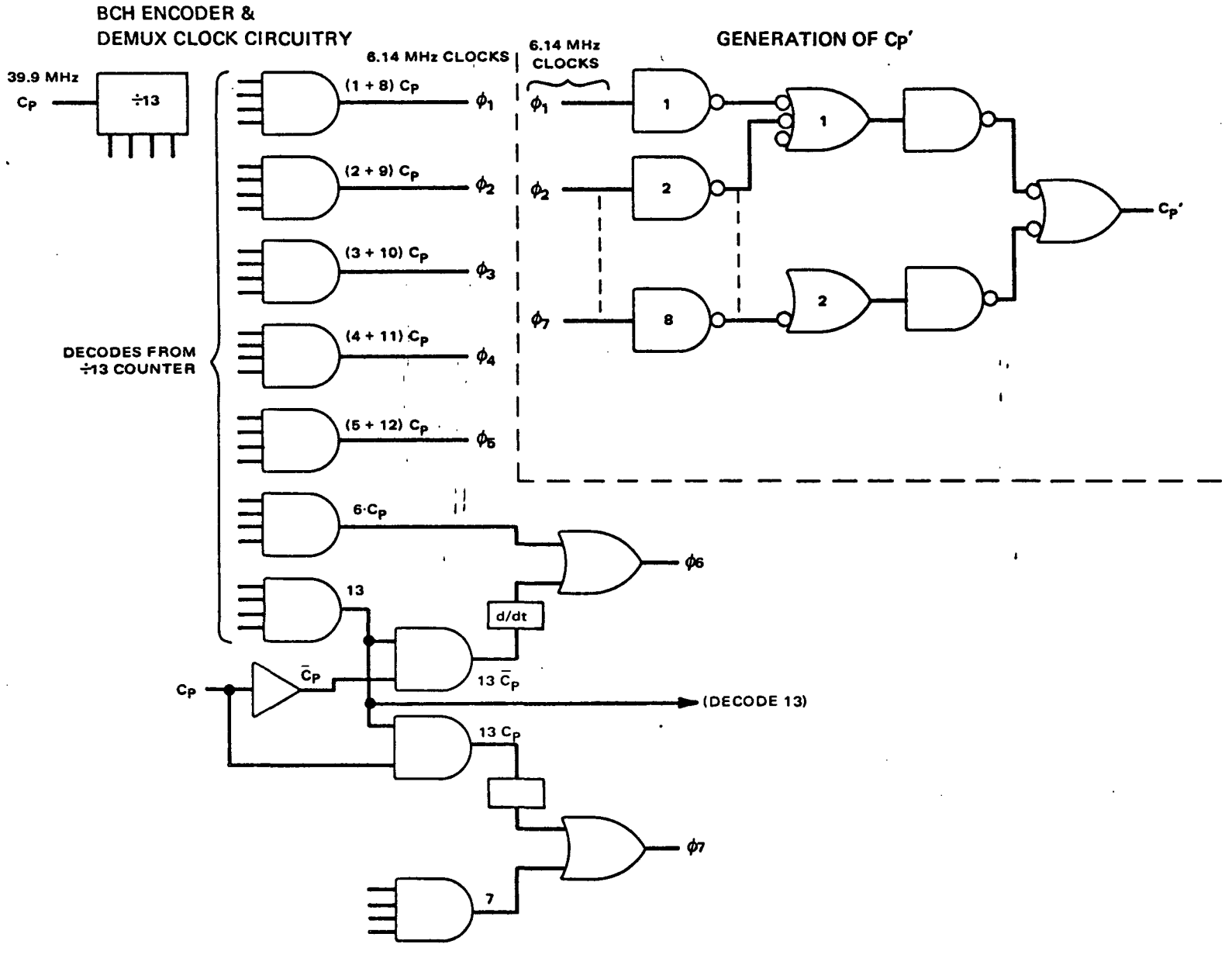


Figure 2-5. Input-Output Clock Logic Circuit (Sheet 1)

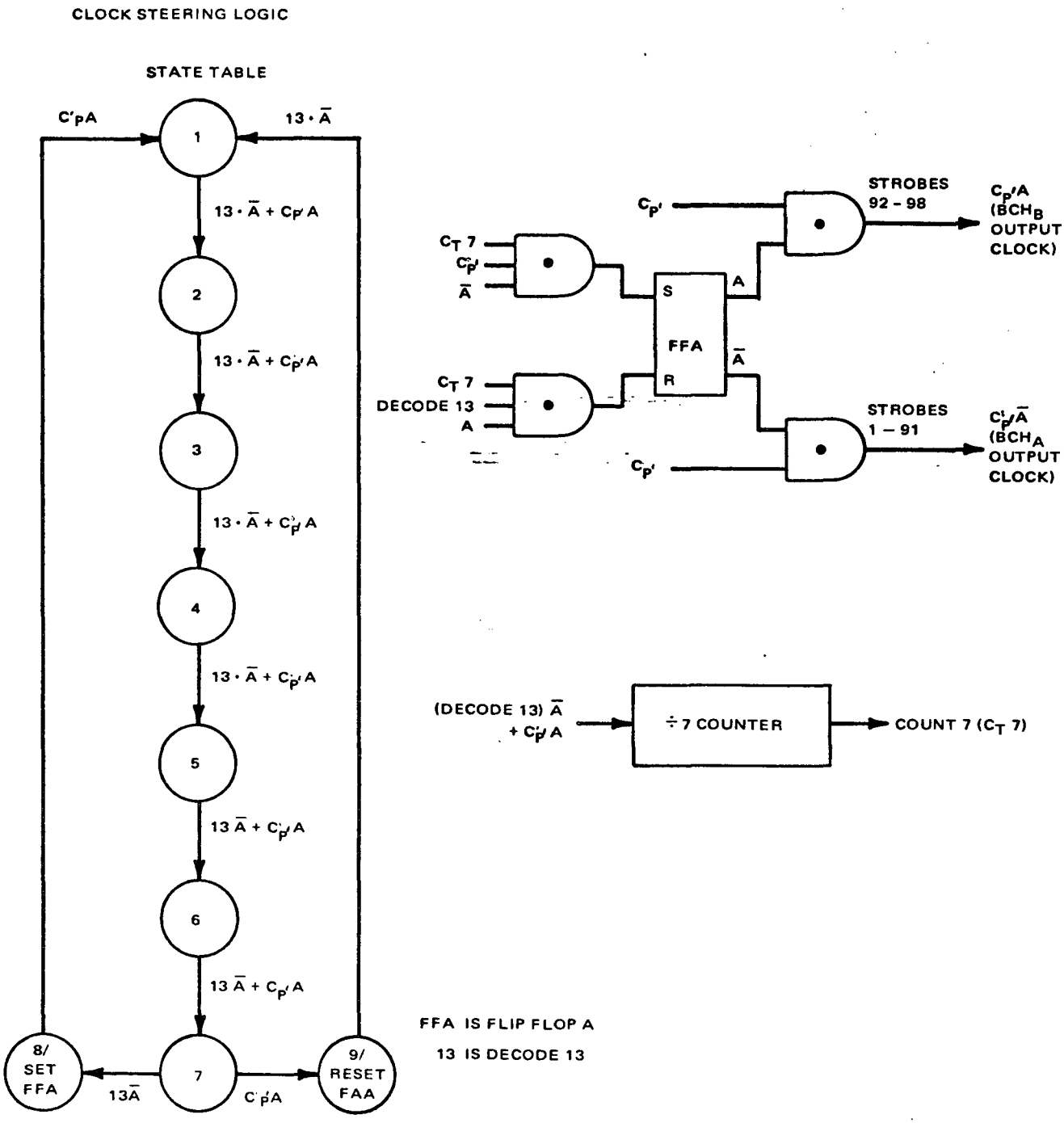


Figure 2-5. Input-Output Clock Logic Circuit (Sheet 2)

55, 56, 69, 70, 83, 84, 97 and 98 have half the time period of all the other bits of the output frame. This is equivalent to clocking the output data at 79.8 Mb/s during those bits, and at 39.9 Mb/s during all other bits in the frame. This portion of the logic circuitry is implemented with the TTL-S (integrated Schottky barrier diode clamped) logic series, which has sufficient speed capability to handle the aforementioned clock rates. An additional advantage of the above clocking scheme is that the output clock is derived directly from the 39.9-MHz input clock, thus eliminating the transient response time that would be associated with a frequency-multiplying scheme using a phase locked loop.

2.1.2.1 BCH Encoder Timing Logic

The BCH Encoder requires 91 clock pulses for BCH_A, followed by seven clock pulses for BCH_B. The logic frame is divided into seven sets of 13 input clock pulses Cp followed by one set of seven Cp. The first seven sets are directed to BCH_A and the last set to BCH_B. For each of the first seven sets, the last input clock pulse Cp 13 is divided into two phases, to provide output clock pulses 13 and 14. These pulses are differentiated to reduce the width of the resultant pulses, and the negative excursion is clamped. The output clock for the BCH encoder is called Cp´. The portion that goes to BCH_A is termed $Cp'\bar{A}$, and the portion for BCH_B is called Cp´A.

The clock-generation logic is shown in Figure 2-6. The input clock waveform Cp drives a ÷ 13 counter. The ÷13 counter is decoded for states 1 or 8, 2 or 9, 3 or 10, 4 or 11, 5 or 12, and states 6, 7, and 13. The resulting decodes are ANDed with the input clock and logically grouped into seven phases, each having a repetition rate of 6.14 MHz. These clocks are used in the multiplexing logic also, and are termed the 6.14-MHz clock phases 1 through 7. The logical relationships between the 6.14-MHz clock pulses and the state of the ÷13 counter are shown below:

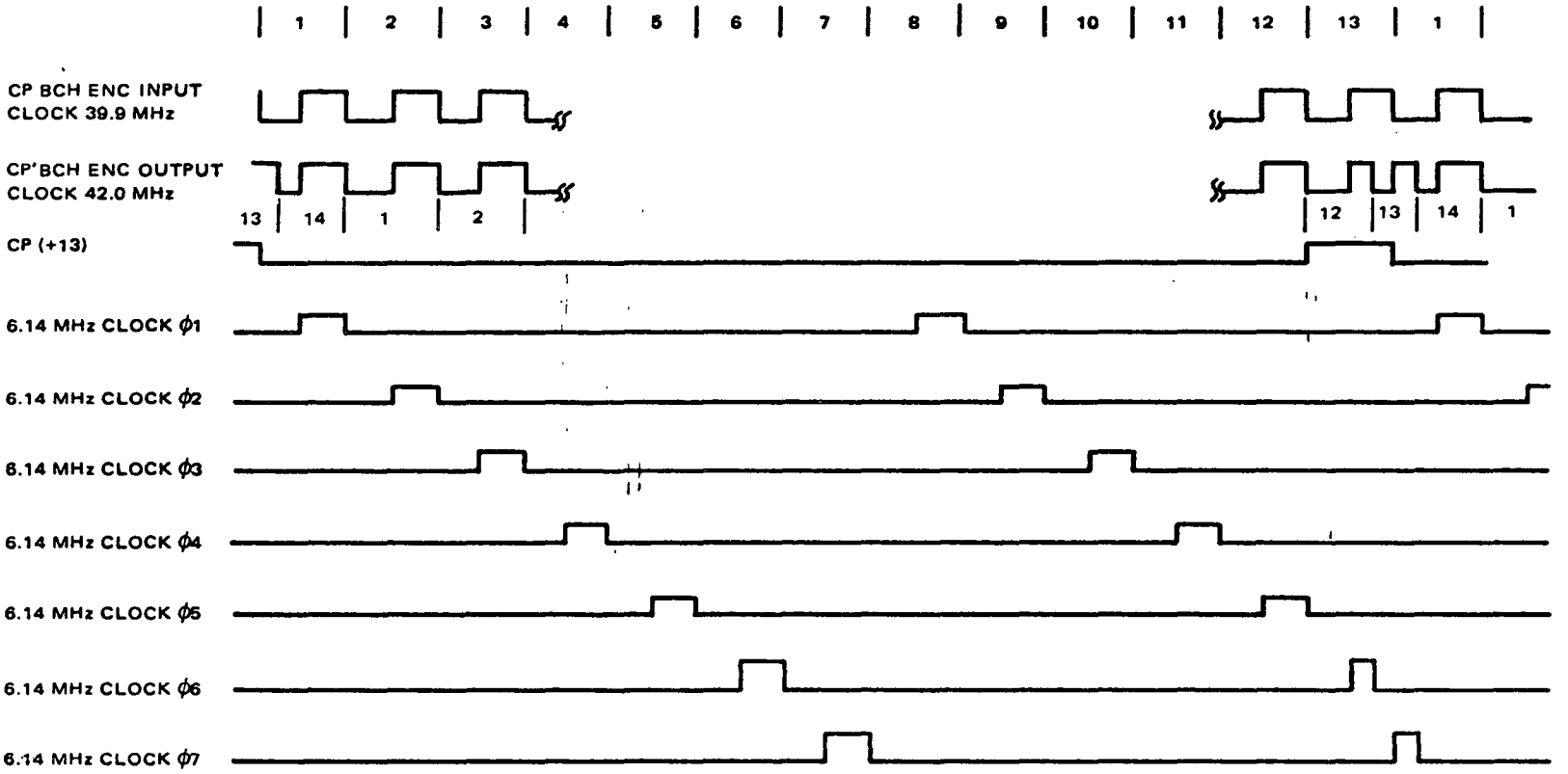


Figure 2-6. Clock-Generation Timing Diagram

6.14 MHz $\phi 1$ = Decode (1+8) $\cdot$Cp

6.14 MHz $\phi 2$ = Decode (2+9) $\cdot$Cp

6.14 MHz $\phi 3$ = Decode (3+10) $\cdot$Cp

6.14 MHz $\phi 4$ = Decode (4+11) $\cdot$Cp

6.14 MHz $\phi 5$ = Decode (5+12) $\cdot$Cp

6.14 MHz $\phi 6$ = Decode 6$\cdot$Cp + (Decode 13$\cdot\overline{Cp}$)

6.14 MHz $\phi 7$ = Decode 7.Cp + (Decode 13$\cdot$Cp)

The bracketed terms connote that the width of the pulse is reduced by the differentiator. The timing diagram for these clock phases is shown in Figure 2-6. The resultant 43-MHz clock Cp´used for the output rate of the BCH encoder is formed by the logical OR of all the 6.14-MHz clock phases, and is shown at the top of Figure 2-6, under the input clock waveform, Cp.

The Logic circuitry for directing the first seven sets of Cp´ (91 clock pulses) to BCH_A, and the last of Cp´(seven clock pulses) to BCH_B is shown on the bottom of Figure 2-5, together with a state table describing the operation of the circuitry. The logic consists of a divide-by-7 counter, and logic to steer Cp´. The divide-by-7 counter at the bottom of Figure 2-5 (Sheet 2) is increment in two modes. When flip-flop A (FFA) is set, the counter advances on each cycle of Cp´. When flip-flop A is reset, the counter advances each time 13 cycles of Cp´ are counted. The 13 cycles of Cp´ are registered by decode 13 from the demultiplexer clock logic, and is indicated by the number 13 on the state table. Flip-flop A changes state each time the divide-by-seven counter makes a complete cycle, CT7. During the time that FFA is reset, 13 sets of seven cycles of Cp´ will be directed to BCH_A, after which, FFA will set, and cause seven cycles of Cp´ to be gated to BCH_B. FFA will then reset and start the next set.

2.1.2.2 Demultiplexing Logic

The scheme for demultiplexing the logic signal out of the BCH encoder consists of three levels of decommutation. The first level divides the 43 Mb/s serial input-data stream into seven parallel paths. Each of these paths is decommutated to two lines, and then finally each of these lines is decommutated into seven lines. A detail of the demultiplexing logic is shown in Figure 2-7. Buffer 1 consists of seven JK flip flops, which are each clocked on the 6.14-MHz clock phases, respectively. The timing diagram of Figure 2-8 shows a complete frame of data and the timing relationships between the data, buffer register 1, and the 6.14-MHz clock phases. The top line represents the 43-Mb/s data stream generated from the BCH encoder. Each bit of the frame is labeled, and it is clear from the data pattern that the frame is composed of seven 14-bit sequences, where each sequence has timing identical with the other sequences. The buffer 1 register data is shown below the 43-Mb/s data stream and the 6.14-MHz clock phases are shown beneath the Buffer 1 register data. Bit 1 of frame n is strobed into B1F1 on the trailing edge of 6.14 ϕ1. Similarly, bits 2 through 7 are strobed into the B1 register flip flops on the other consecutive 6.14-MHz clock phases. During the period of bit 8, the contents of the buffer register, which is the first seven bits of the frame, is clocked into the next level buffer, on a 3.075-MHz phase A strobe. Simultaneously Bit 8 of the frame is strobed into B1F1 again with the 6.14-MHz ϕ1 clock. As before, during the period of bit 15, bits 8 through 14 of the frame are stored in the buffer 1 register. This portion of the data is strobed into the next level of buffer on a 3.075-MHz phase B strobe. This process is continued through the entire frame, until all 98 bits are processed. The same operation is repeated for all succeeding frames.

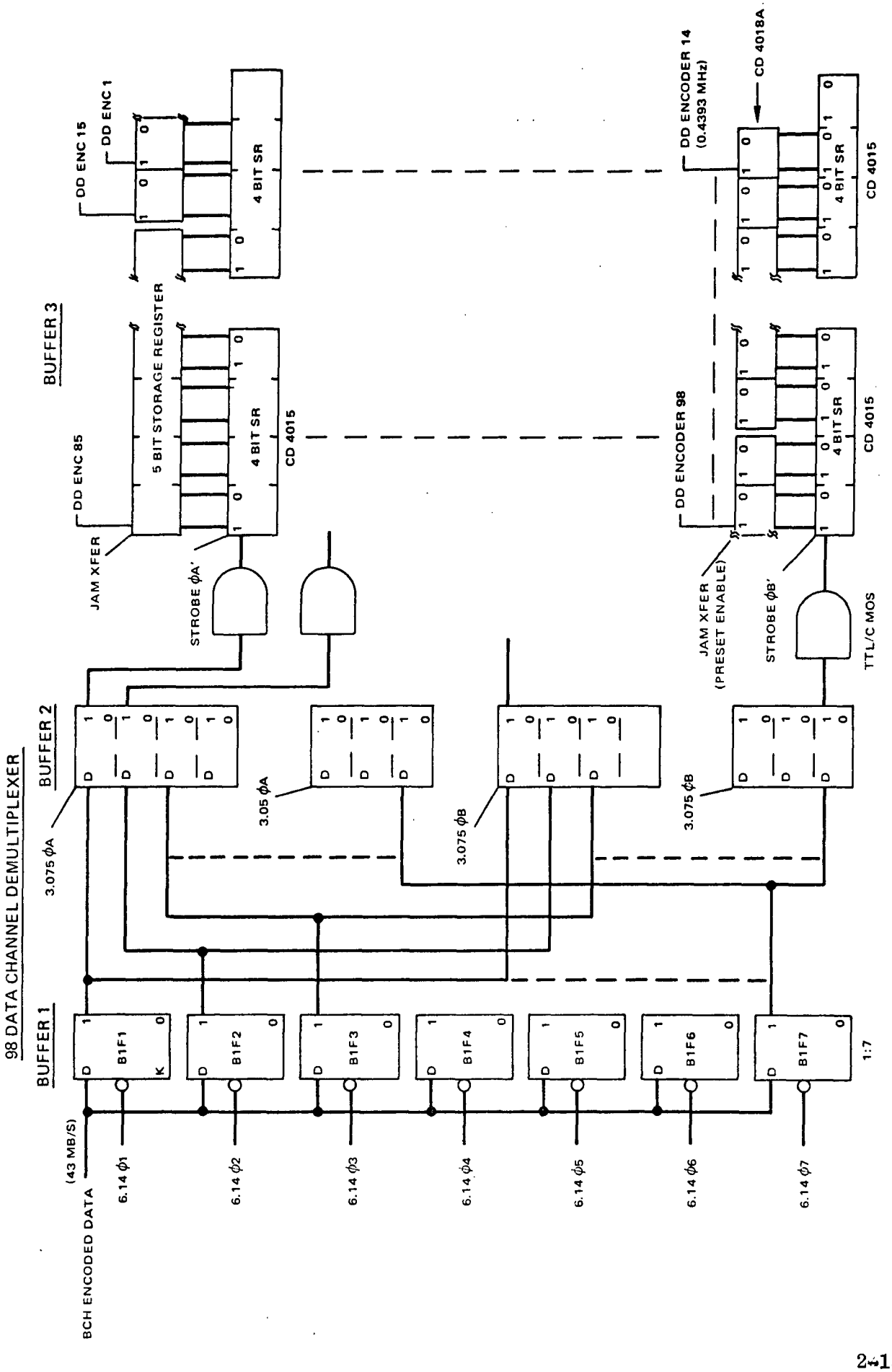
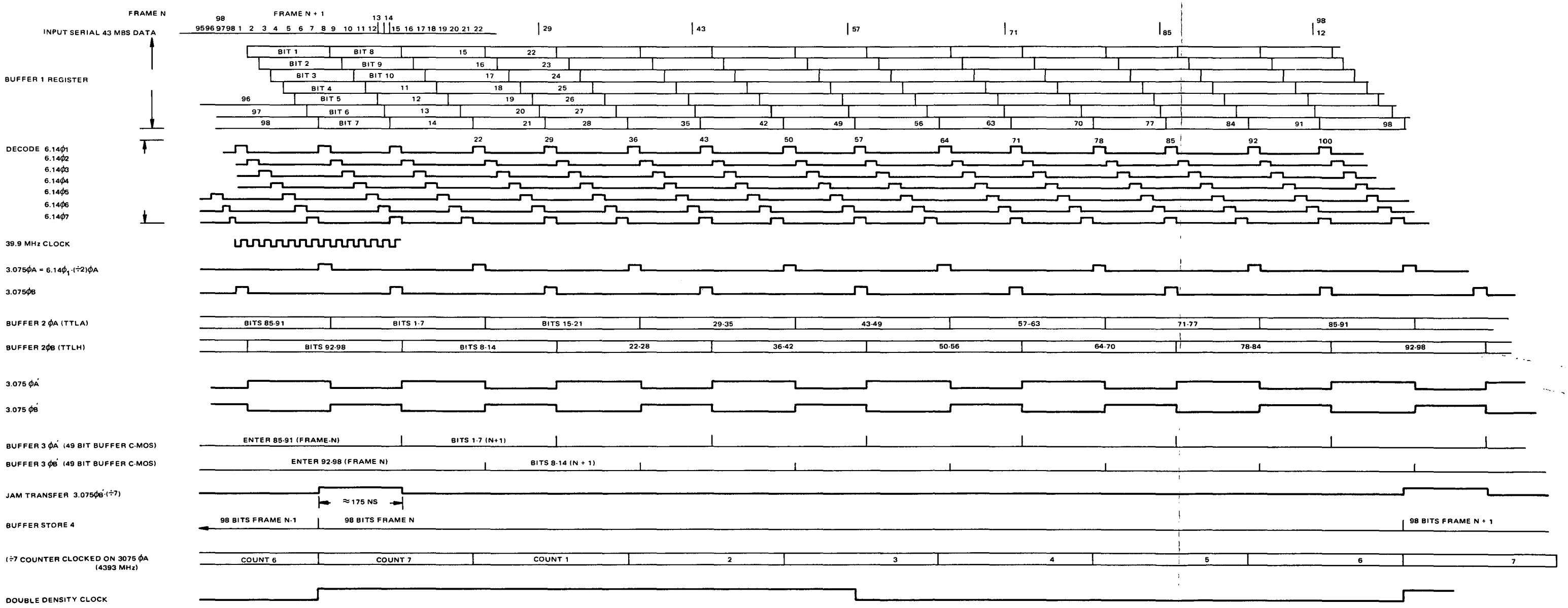


Figure 2-7. 98 Data Channel Demultiplexer, Logic Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2



2-17/2-18

Figure 2-8. Demultiplexer Timing Diagram

The buffer 2 register consists of 14 flip flops, seven of which are clocked on the 3.075-MHz ϕB strobe. These strobes are derived from the 6.14-MHz ϕ1 clock. The two phases of the 3.075-MHz clock are not centered at exactly 180 degrees apart, because two of the bits that are loaded during the phase B strobe are shortened. The data storage for the Buffer 2 register is shown on the timing diagram. The period of overlap between the two phases of data storage (for examples Bit 1 through 7, and Bit 8 through 14) is 176 ns. During this period, the 14-bit contents of the buffer 2 register is clocked into the 3 level of demultiplexing. The clock for this level is an assymetrical square wave at a repetition rate of 3.075 MHz. This clock and its complement is derived from the 3.075-MHz ϕA and ϕB strobes, and is labeled 3.075 ϕA´ and 3.075 ϕB´, respectively.

The third level of multiplexing consists of a set of serial shift registers and a set of storage registers. The outputs of this level drive the double density decoders, which interface with the record electronics of the tape recorder. The data transfers from level 2 occur on alternate phases of the 3.075 ϕA´ and 3.075 ϕB´ clocks. There are seven ϕA´ and ϕB´ transfers per frame, and each of the ϕA´ and ϕB´ clocks transfer seven bits of data, comprising a total of 98 bits per frame. To accommodate the format of the data transfer, the input section of buffer 3 has 14, seven-bit, serial shift registers. After seven ϕA´ and ϕB´ transfers, starting from point A on the timing diagram, the serial shift registers will contain all the data bits in the frame. Since the buffer 3 serial registers are loaded on alternate clock phases, the period of time during which the serial registers contain the full data frame exists for approximately 175 ns. During this time, the entire contents of the serial registers is transferred to the storage registers using the parallel transfer (PT) pulse. The PT is derived from

the 3.07-MHz $\phi A'$ clock using a $\div 7$ counter and combinational logic. The data transfer is effected on the leading edge of PT and occurs once per 98 data bits.

2.1.2.3 Double Density Encoder

The ability to record PCM data in a record system is restricted by limitations in the parameters of system bandwidth, time-base stability, and signal linearity. NRZ-L data encoding requires a system frequency response to dc in addition to good phase linearity. Failure of the system to meet these requirements results in baseline distortion that makes the further processing of playback data more difficult. Since the data clocks are derived from the data, the time-base stability of the recorder impacts the playback circuitry that handles the extraction of the clocks, as well as the data. Encoding the data with biphase data eliminates the requirement for system frequency response to dc, but also extends the upper frequency bandwidth requirements to approximately 1.8 times that of NRZ(L) data.

Double-Density encoded data, has the advantage that the upper-frequency system requirements are the same as that for NRZ(L) PCM, while the low-frequency response requirement is much less than that required for NRZ(L). The power spectral density vs. frequency plot of these forms of encoding is shown in Figure 2-9. The algorithm for double density encoding can be defined as follows: An NRZ-1 is represented by the transition in the middle of a bit cell,and an NRZ-0, followed by an NRZ-0, is represented by a transition at the end of the first zero's bit cell.

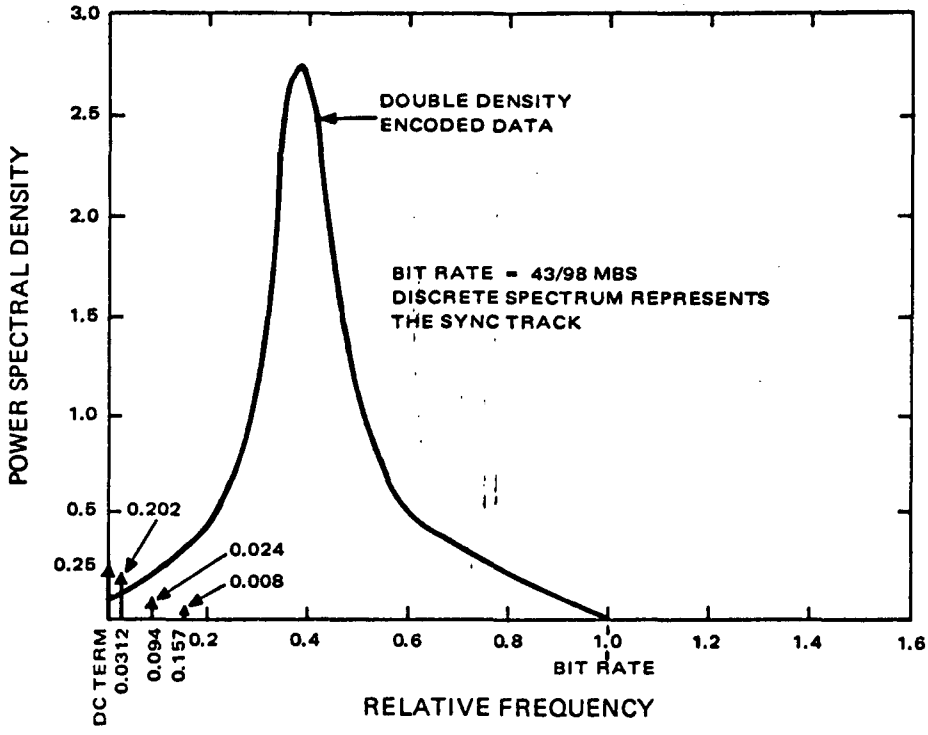


Figure 2-9. Double Density Encoded Data Power Spectral Density, With Sync Signal Spectral Density Waveform.

The implementation of the DDE data is shown in Figure 2-10. The NRZ data input is driven from the output of the third level of multiplexing at 43/98 Mb/s and the double-density clock is decoded from the record timing logic. There are 98 double-density encoders and each one is implemented with a modulo-2 adder and a D-type flip-flop. Because of the number of circuits required and the low data rate, C-MOS circuits are used for the implementation.

2.1.2.4 Sync Track-Skew Marker Signal

The sync track waveform is a square wave which repeats every 32 data bit periods. There are seven sets of 2 parallel sync tracks evenly spaced across the tape. Two adjacent tracks are used to provide redundancy in the event one of the tracks is disabled by a failure. The sync track signal is derived from the double-density encoder clock by using the output of a five-stage binary counter. Since the output of the counter is synchronous with the double-density encoder clock, the transition in the sync track signal from one logic level to the other resolves the DD encoder timing ambiguity because it locates the start of a data bit edge. The sync track signal is recorded on all sync tracks simultaneously. Hence, the amount of relative displacement from one transition to the next indicates the relative skew occurring in the tape during playback.

2.1.2.5 Synchronization Signal Power Spectral Density

The sync track signal is a square wave whose repetition rate is one-thirty-second that of the data bit rate. The sync track is therefore, 1/32 x 43/98 MHz, or approximately 13.7 kHz. Since the synchronization signal is a repetitive square wave, the power spectral density distribution will be composed of the discrete terms of the Fourier series expansion of the sync signal. The Fourier series expansion for the sync signal of unity height is given as:

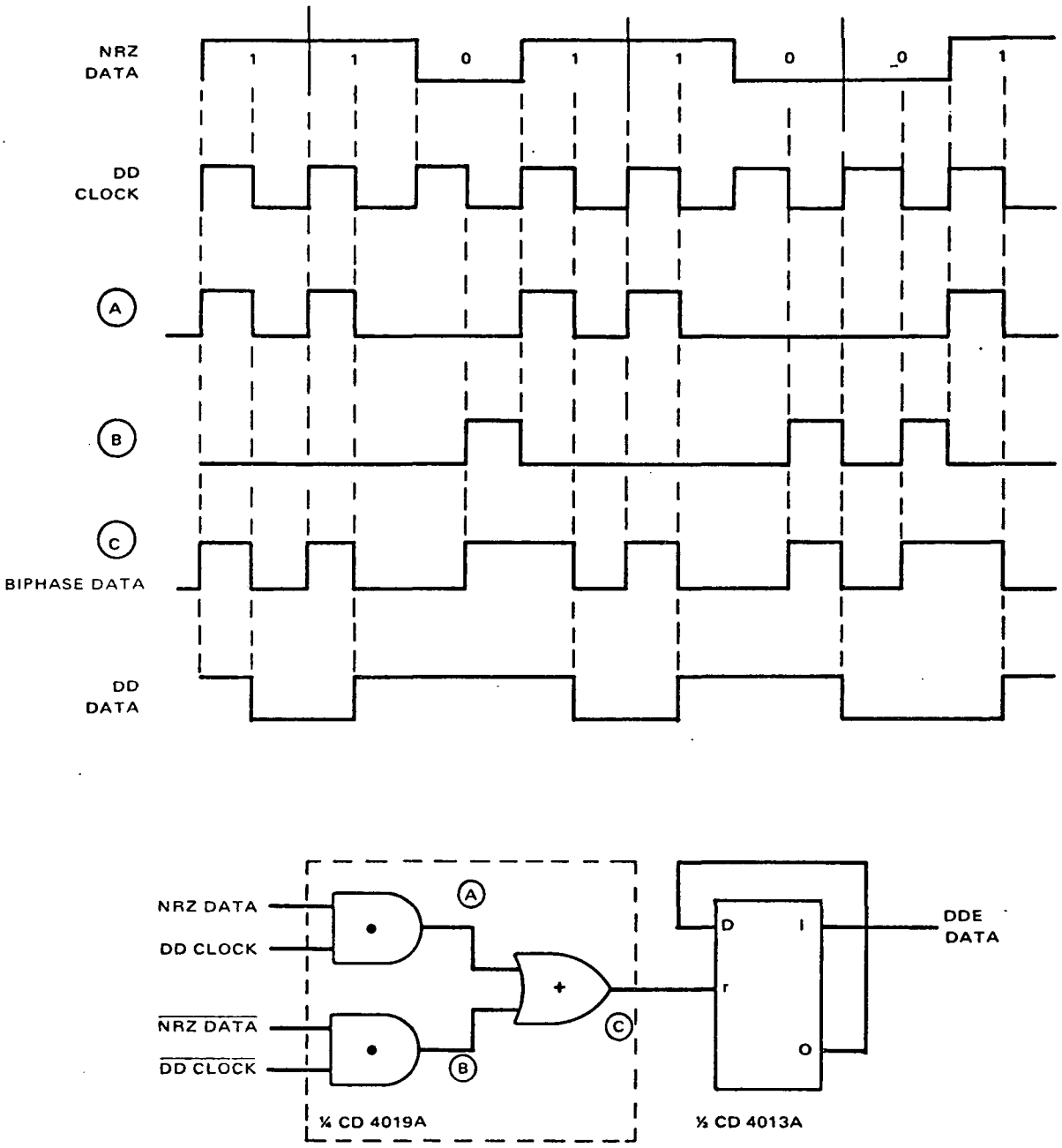


Figure 2-10. NRZ to DD Encoding

$$f_{sync(t)} = 1/2 + \sum_{n=0}^{\infty} \sqrt{2} \left(\frac{\sqrt{2}}{\pi} \frac{(-1)^n}{2\ n+1} \right) \cos\ (2\ n+1)\ f\ t$$

where F is the sync signal repetition rate of 13.7 kHz.

In the above expansion, the rms value of each term is given by the bracketed term in the amplitude factor. The distribution of power and frequency is given in Table 2-1 and the results are plotted in Figure 2-9.

TABLE 2-1. SYNC SIGNAL POWER DISTRIBUTION VERSUS RELATIVE FREQUENCY

DC Term	Relative Power at Each Frequency Component	Frequency	Relative Frequency
-	0.25	DC	DC
0	0.202	f_{sync}	1/32 of bit rate
1	0.024	3 f_{sync}	3/32 of bit rate
2	0.008	5 f_{sync}	5/32 of bit rate
3	0.004	7 f_{sync}	7/32 of bit rate
n	$\left(\frac{\sqrt{2}}{\pi} \frac{(-1)^n}{2N+1} \right)^2$	(2n+1) f_{sync}	(2n+1)/32 of bit rate

2.1.3 Playback Electronics

Clock and synchronization tracks are recorded on the MCTR channels as follows:

DATA TRACKS*	SYNC TRACKS
1-7	8, 9
10-23	24, 25
26-39	40, 41
42-55	56, 57
58-71	72, 73
74-87	88, 89
90-103	104, 105
106-112	

*Data tracks are also used for capstan motor servo.

The sync information is redundantly recorded on adjacent tracks so that a single failure affecting a sync track does not impair the ability to reconstruct the recorded data. The proposed sync track signal is a squarewave, repeating every 32 bits. A basic clock at twice the data rate is required for converting the data from Double Density Encoding to NRZ(L), prior to deskewing and multiplexing the data. The clock recovery circuitry consists of seven phase-locked loops. The basic timing for the data and the PLL is shown in Figure 2-13. The maximum tape skew across the entire width of the tape is one μm (40 μin). At a tape-packing density of 0.8 Mb/m (20 kb/in.), this corresponds to a maximum differential displacement of 0.8 bit across the entire tape. Each two redundant sync tracks are "OR'd" and used to drive one phase-locked loop.

The phase differential between adjacent sets of clock tracks is proportional to the tape skew. Since the maximum displacement across the tape is 0.8 bit, the maximum displacement per track is 0.00714 bit, and over a block of 14 tracks, the displacement will be 0.9996 bit. The clock used for the double density decoders and the deskew circuitry is derived from the phase-

locked loops and these are synchronized to data tracks flanking each set of sync tracks, midway between each block of 14 tracks.

In the following description, when data tracks are discussed, they will be referred to as numbered 1 through 98. When the sync tracks are discussed, the tape track locations will be specified and the words "sync tracks" will be used to avoid ambiguity. This also makes it easier to visualize, because once the sync tracks are removed, the remaining data tracks appear as 98 parallel data streams. After the clocks are recovered and the sync sequences detected, the data is converted from double density encoded format back to NRZ(L). A buffer is used to electrically remove any skew and jitter from the tape and to reclock the data to a stable system clock. The data is then time-division-multiplexed by the use of a parallel-to-serial converter. The output format is two serial 64.58-Mb/s signals having a constant differential delay of one-half data bit between them.

2.1.3.1 Playback Electronics Block Diagram

A block diagram of the playback electronics is shown in Figure 2-12. Each of the playback signals is equalized and limited to provide uniform signals over the frequency range of the system. Clock information to drive the Double Density Decoders and the deskew buffer is derived from the data tracks adjacent to the sync tracks, using phase-locked loops. The phase-locked loops are used to provide a clock that is synchronous with the data and to provide a clock during tape dropouts. The data, as read from the recorder, is Double Density Encoded PCM. This is converted back to NRZ, and then processed in the deskew buffers. The deskew buffers are long enough to compensate ±4 bits of skew relative to the center clock track of the tape recorder. The resulting output from the deskew buffer is the NRZ encoded data, in the form of 98 parallel channels and at

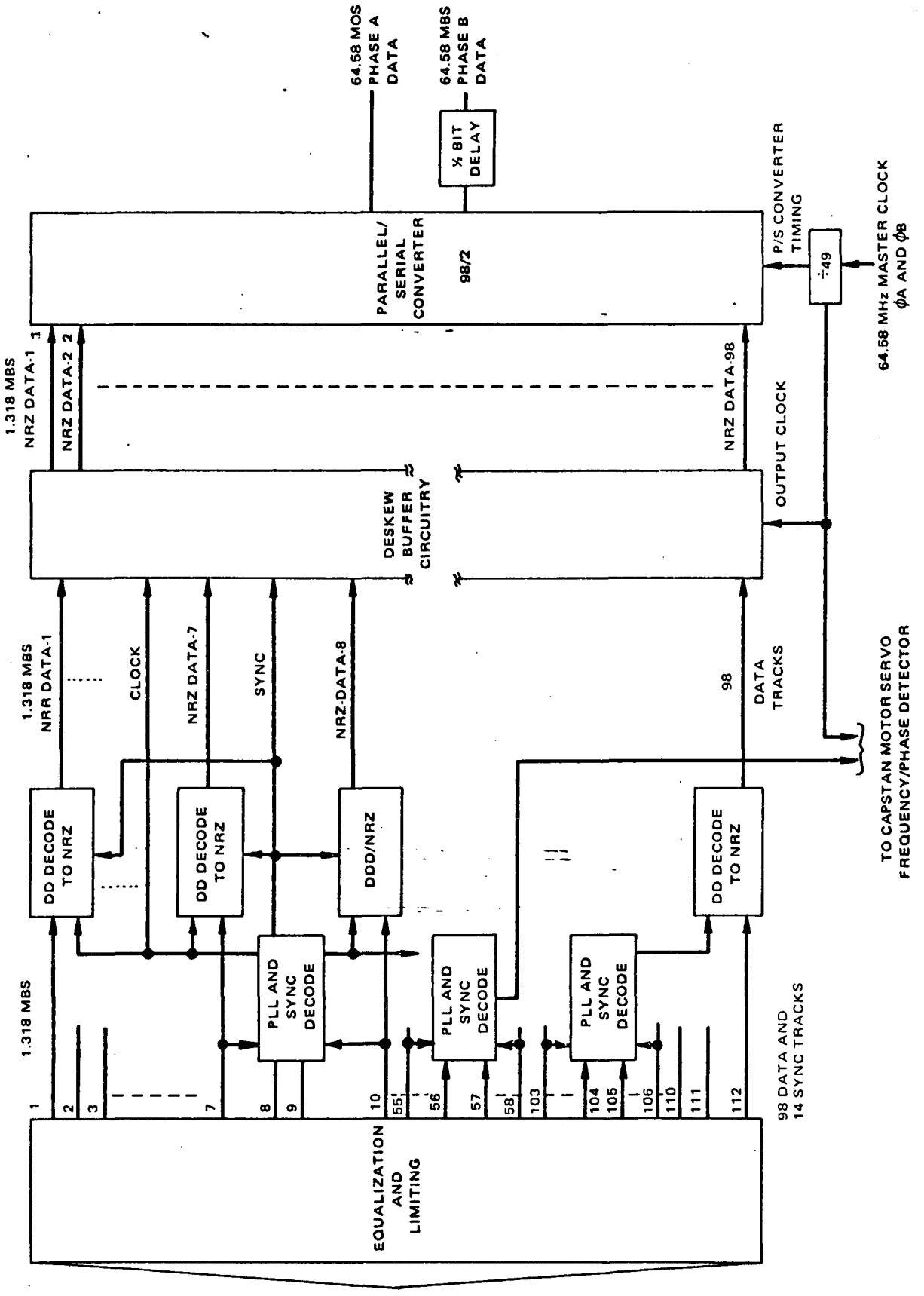


Figure 2-12. MTR Playback Electronics, Block Diagram

a bit rate of three times the record rate or 1.318 Mb/s, with all skew removed from the signal. A parallel-to-serial converter converts the 98 parallel input signals to two serial bit streams at 64.58 Mb/s. These streams are used to modulate a four-phase transmitter. The four phases are derived by delaying one phase by a half bit period relative to the other phase. The playback speed is controlled by phase-frequency locking the clock derived from the center data tracks (55, 58) to the 64.58-MHz master playback clock.

2.1.3.2 Phase-Locked Loop; Reference Signal

Bit timing information in the playback signal is carried in the data transitions, which mark the 0- and 180-degree points of the double-density encoded data. Transitions have either positive or negative direction, but both carry the same timing information for clock recovery. If these transitions are converted to a series of undirectional pulses, a spectral component at twice the bit frequency will be generated which the loop can be locked to. Figure 2-13 illustrates one method of clock recovery together with typical timing waveforms. The input data signal is passed through a delay circuit and then both the delayed signal and the original signal are applied to an exclusive-OR gate. The resulting output from the exclusive-OR gate is a series of unidirectional pulses, which occur at 0^{o} and 180^{o} points in the bit period and have a pulse width equal to the signal-propagation delay through the delay circuit. This exclusive-OR output signal (EOO) is used as the reference input to the phased-locked-loop (PLL) phase detector. The input to the PLL therefore, has a strong spectral component at twice the data bit rate, a constant width, and a logic level amplitude.

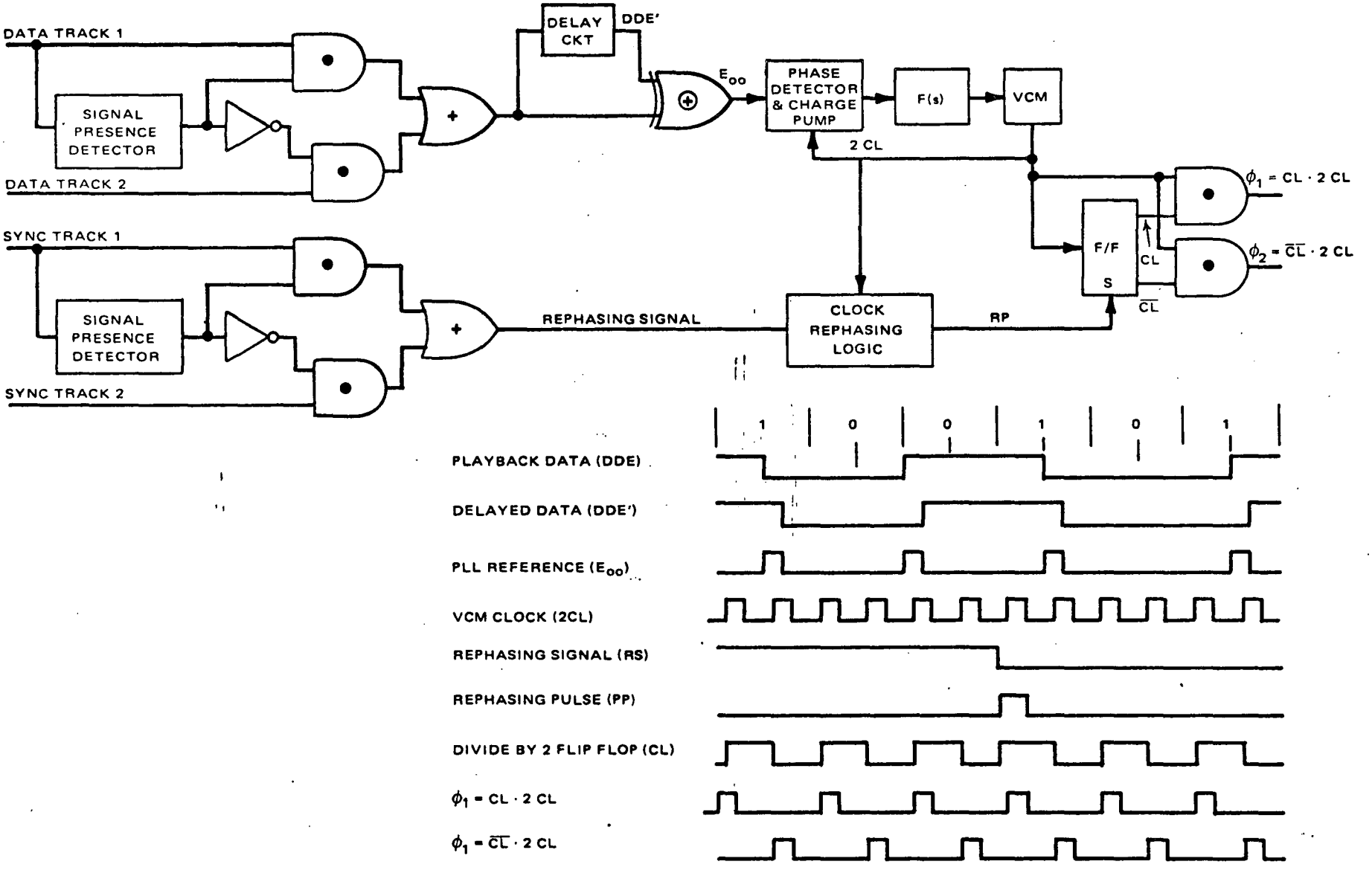


Figure 2-13. Clock Recovery Timing Diagram

2.1.3.3 Phase-Locked Loop; Phase Detector

The proposed PLL phase detector is the charge pump circuit shown in Figure 2-14. The timing diagram associated with this circuit is shown in Figure 2-15. The function of the phase detector is to compare the voltage-controlled-multivibrator (VCM) leading clock edge with the window EOO derived from the playback clock track. The phase-detector output voltage VA is proportional to the displacement of this clock edge from the center of the window. During the acquisition mode, the VCM output frequency will slew over the pull-in range of the loop. Eventually the clock edge will fall within the EOO window. For the period of time that the VCM output is low and the window is high, charge will be removed from the capacitor, and during the time that both VCM and EOO are high, charge will be added. The parameters of the circuits are adjusted such that at lock, the output voltage VA will be at nominal mid-range.

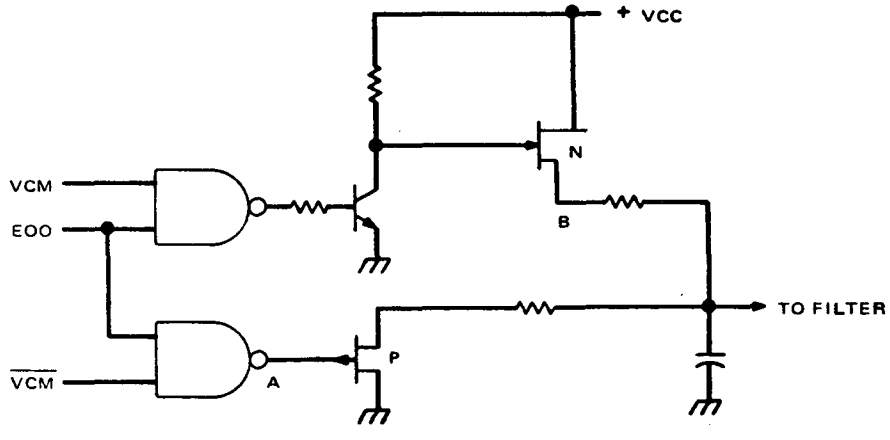
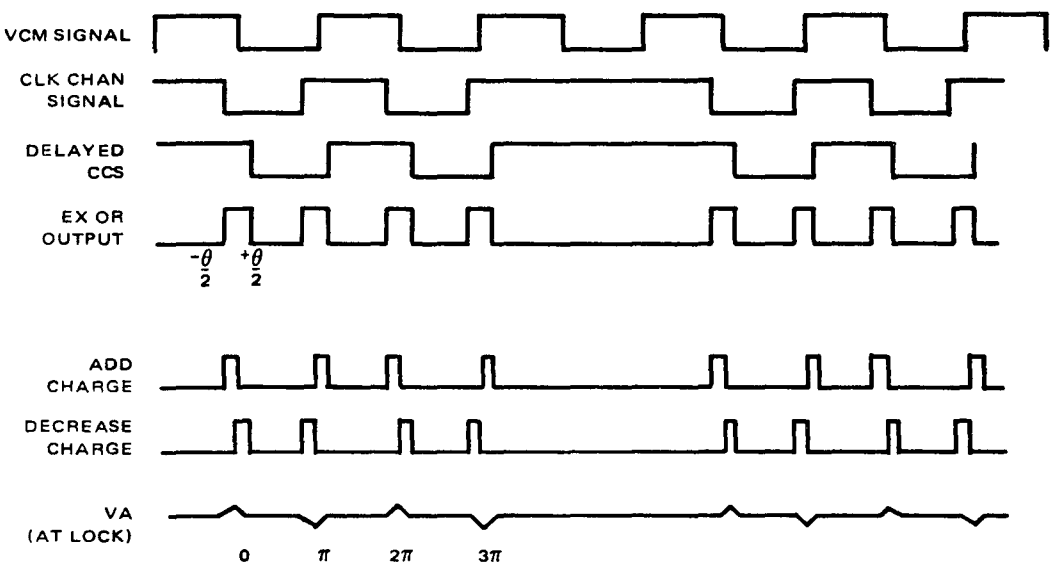


Figure 2-14. Phase Detector Circuit



NOTES: 1. θ = PORTION OF VCM CYCLE WHEN EOO REFERENCE OCCURS
2. VA = AVERAGE PHASE DETECTOR OUTPUT VOLTAGE
3. RELATIVE PHASE IS PHASE OF VCM MINUS PHASE OF EOO WINDOW
4. THERE ARE TWO EQUILIBRIUM POINTS PER 2π RADIANS OF PHASE OFFSET BETWEEN THE VCM AND THE REFERENCE:
   (1) WHERE OUTPUT SLOPE IS NEGATIVE, THESE OCCUR AT EVEN MULTIPLES OF 2π RADIANS AND ARE STABLE EQUILIBRIUM POINTS.
   (2) WHERE OUTPUT SLOPE IS POSITIVE.

Figure 2-15. Phase Detector Pump Circuit; Timing Waveforms

2.1.3.4 Phase-Locked Loop; Loop Filter

The requirement of the loop to provide a continuous clock locked to the data rate dictates that a second-order, phase-locked loop be used. In the second-order loop, the frequency information is stored in the form of charge on the integrator driving the VCO. When the input signal drops out, the loop opens and the integrator discharges with an RC time constant. Using an active loop filter of the type shown in Figure 2-16 changes the decay time to A R_1C. In an active loop, A can be made very large, insuring that the VCO output frequency will not change appreciably during the synchronization sequence. The transfer function for this type of loop filter, for large amplifier gain is given as

$$F(s) = \frac{s\ R_2C + 1}{S\ R_1C} .$$

The time constants R_1C and R_2C,

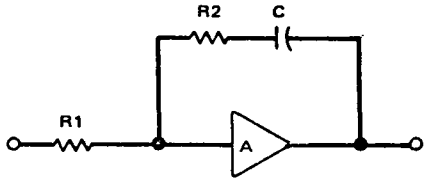


Figure 2-16. Phase-Locked-Loop Filter

together with the phase detector, and VCM gain constants, determine the natural frequency and the damping factor of the loop, which in turn determines the loop bandwidth and transient response. The loop filter can be implemented using monolithic operational amplifiers and discrete components.

2.1.3.5 Voltage Controlled Multivibrator (VCM)

The loop clock, which is phase locked to the input clock signal, will be implemented using a monolithic multivibrator, the MC4324F. The center frequency is determined by an external capacitor and the output frequency is variable over a 3.5-to-1 ratio with a -1-volt to +5-volt range on the dc control input. The VCM provides a buffered output and is packaged with two circuits to an IC package.

2.1.3.6 Clock Synchronization Circuitry

Two phases of clock signals at the bit rate are required for the Double Density decode circuits. These clock phases are derived from the VCM, which has a square-wave output frequency at twice the bit rate. This results in a phase ambiguity in the DD decode clock, which must be resolved for proper decoding. The phase ambiguity is resolved in the clock rephasing logic shown in Figure 2-13. The resynchronization pulse R_p operates as a flywheel type reset, in that the phasing flip-flop (Figure 2-18) does not require the rephasing pulse to maintain proper phasing of $\phi 1$ and $\phi 2$. The rephasing pulse is only used to initially establish $\phi 1$ and $\phi 2$ and to restore the timing if synchronization is lost.

2.1.3.6a Signal Redundancy

Because each set of 14 data tracks are clocked from data derived from the phase-locked loop, redundancy is provided to preclude a loss of one track (the one from which the clock is derived) from causing the loss of the other 13 data tracks. Redundancy is provided in the provision of both the phase-locked-loop reference signal, and in the synchronization track signal. Figure 2-13 depicts the redundancy circuitry for both of these signals. The circuitry uses circuits called "signal presence detectors", which cause the phase-locked loop and

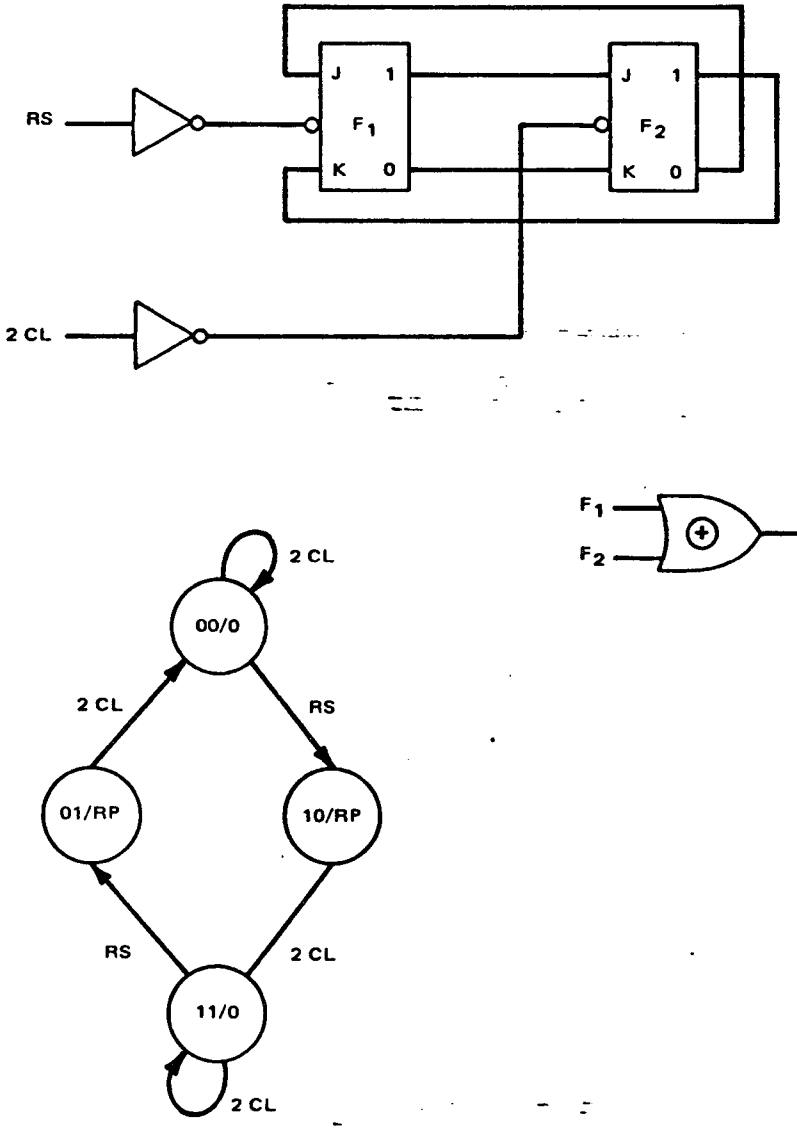
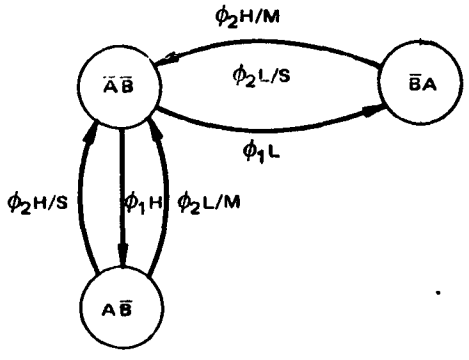


Figure 2-17. Clock Rephasing State Diagram

synchronization circuitry to normally be driven from data track 1 and sync track respectively. In the event of a recorder head failure (or tape drop-out etc.), control would be automatically switched to either data track 2, or sync track 2. Redundancy of this type is provided for all of the phase-locked loops; hence, seven circuits of the type shown in Figure 2-13 are provided. In the event of a data track dropout, some data may be lost until the phase-locked loop locks to the new data track input. In the event the synchronization signal drops out, there should be no data loss because the synchronization signal is only used to establish the double-density decoder-clock phases, initially, and then provides phasing information, in case synchronization is lost.

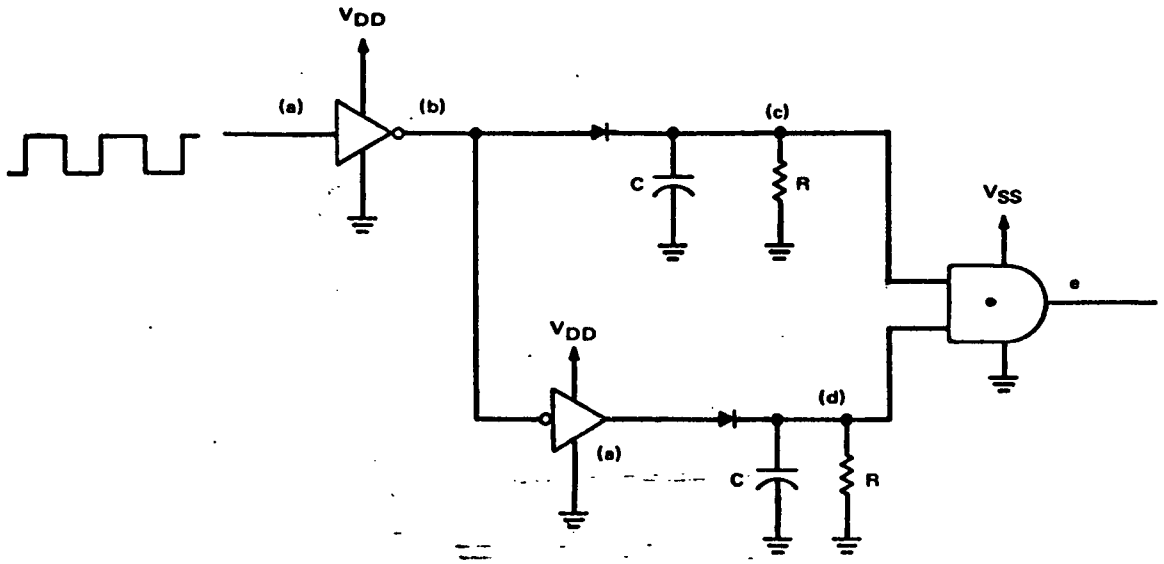
2.1.3.6b Signal Presence Detectors

The signal presence detector is used in both the redundant data-track, and the redundant sync-track switching circuits. As long as a time-varying signal is present at the detector input, the output level remains at a constant logic 1 level. If the input to the signal presence detector remains at a constant level, either a constant logic 1 or a constant logic 0, the output will go to the logic 0 state after a predetermined period of time. There are various ways to implement a circuit of this type. One possible implementation is shown in Figure 2-18A. The waveforms shown are for the case where the input becomes a constant 1. As long as the input is being driven, the capacitors are periodically charged to the full logic-gate output voltage V_{DD}. When a constant 1 is applied, point (b) drops to the gate's low output voltage level V_{ss}, and point (c) will decay towards that voltage at a rate determined by the RC time constant. When the voltage across the capacitor crosses the threshold level of the AND gate, the output of the AND gate will go to logic zero, indicating that the input is no longer present. Similar waveforms result for the case where a constant logic 0 input is applied.



DD ENCODED DATA = HIGH LEVEL = DA
DD ENCODED DATA = LOW LEVEL = $\overline{DA}$
MARK SPACE = M
SPACE PULSE = S
ϕ_1 = PHASE 1
ϕ_2 = PHASE 2

Figure 2-18. Decoding Logic Development



WAVEFORMS FOR SIGNAL PRESENCE DETECTOR

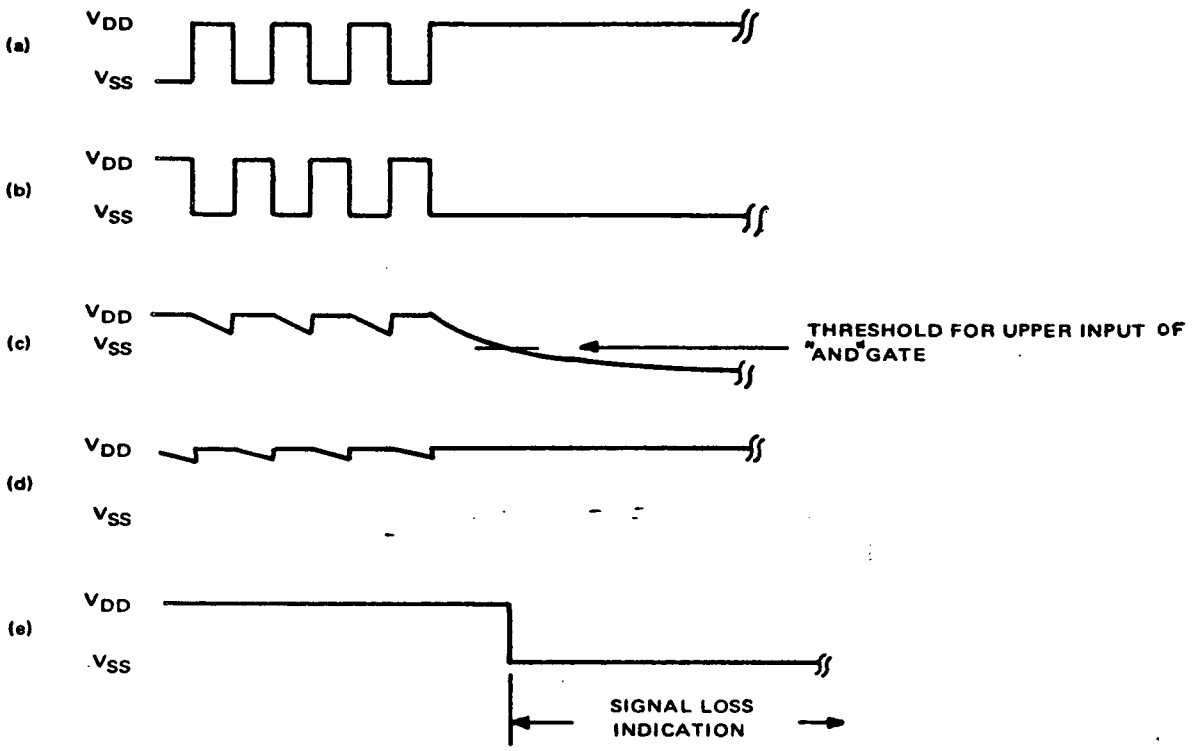


Figure 2-18A. Signal Presence Detector Circuit and Waveforms

2.1.3.7 Double Density Decoder

The Double Density Decoder is used to convert the playback data to NRZ(L) format. The Playback Data is strobed during the first half of a bit period with a $\phi 2$ clock. The decoding algorithm is as follows: A change in level during a bit period corresponds to a NRZ "mark" data bit, and the absence of change in a bit period corresponds to a NRZ "space" data bit. The logic development for this decoding scheme outlined in Figure 2-18.

The implementation of this state table results in a circuit using three C-MOS flip-flops and some combinational logic. The circuit is shown in Figure 2-19, together with typical timing waveforms. As shown in the timing waveforms, the resulting NRZ(L) encoded data has bit edges concurrent with clock $\phi 2$. Thus, the NRZ(L) data lags the double density encoded waveform by half of a bit period.

2.1.3.8 Dejitter-Deskew Buffer Logic

The Dejitter-Deskew Buffer is a digital logic circuit that provides the means for removing the skew added to the data channel phasing by the tape transport. There are 98 separate Dejitter-Deskew Buffers, one for each data channel. The output of the Buffers is a parallel 98-bit output, where each bit is in phase with all the other bits. The basic concept of the Dejitter-Deskew Buffer is presented in the following discussion, followed by a scheme for implementing the Buffer.

The Buffers are composed of circulating registers with separate data read-in and data read-out logic. The data read-in logic timing for each group of 14 data channels is controlled by the data clock derived from the PLL (shown on the bottom of Figure 2-19, Sheet 1) centered in each group of 14 data channels. Thus, there are seven different read-in clocks, one for each

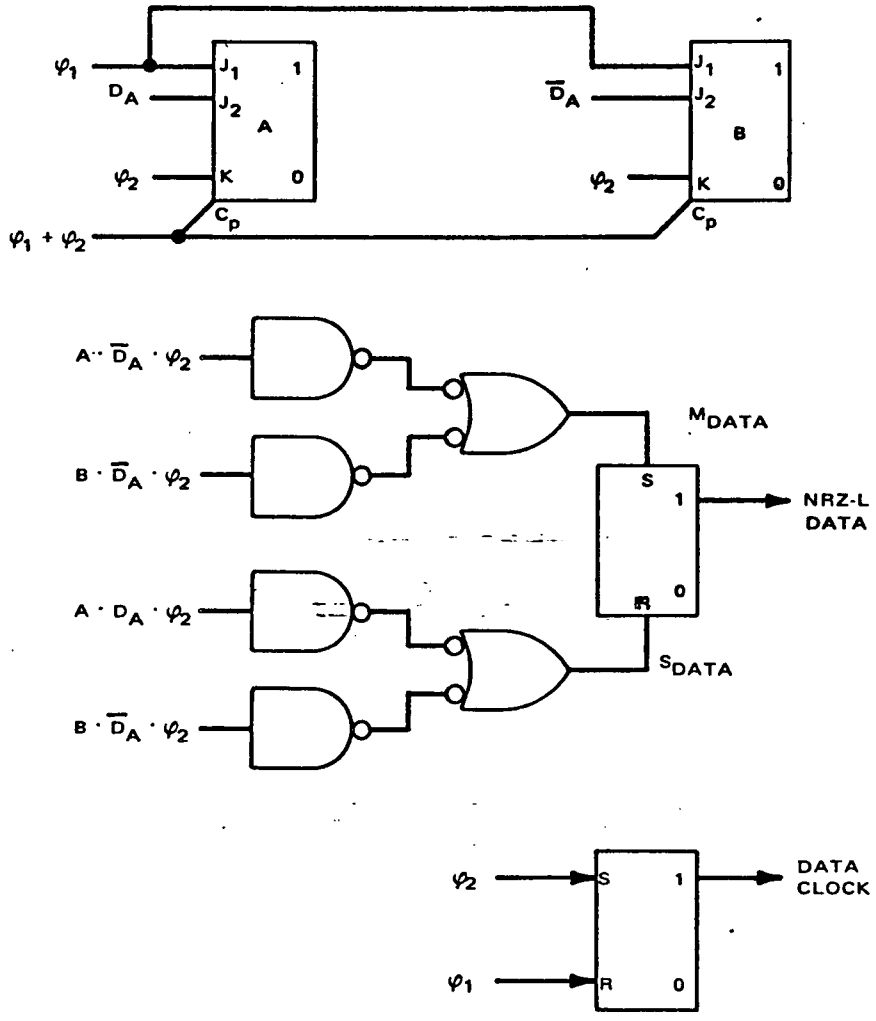


Figure 2-19. Double Density Decoder Implementation and Timing Waveforms (Sheet 1)

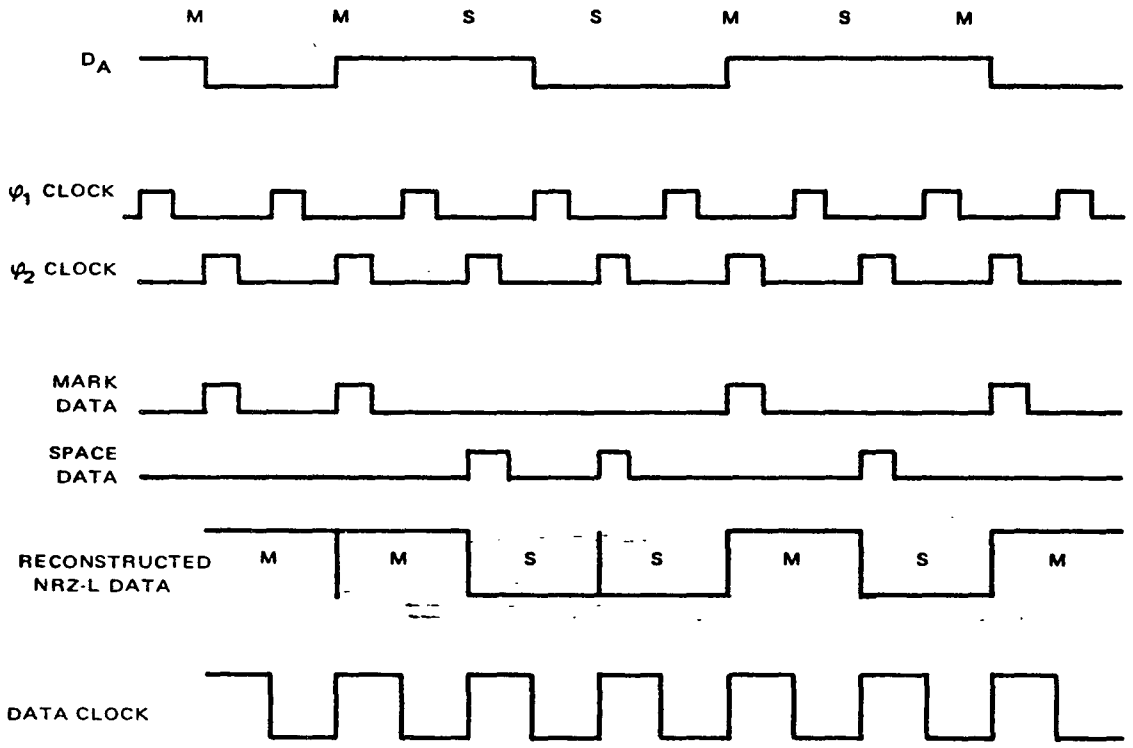


Figure 2-19. Double Density Decoder Implementation and Timing Waveforms (Sheet 2)

group of 14 data channels on the tape. The read-out clock timing is derived from the master system clock and is common for all the Dejitter-Deskew Buffers. Thus, the circulating register must contain enough storage so that under the worst-case conditions, there is always a net minimum displacement between the read-in and read-out positions in the Buffer. A preliminary necessary condition for the successful operation of the Buffer, as presently configured, is that the maximum displacement across 14 data tracks is small enough so that all 14 tracks can be clocked from the pair of clock tracks located at the center of the set. This means that the maximum displacement due to skew across 14 data tracks is small enough that all 14 tracks can be clocked together from a clock derived from the center tracks without the need for performing any additional data buffering on the data streams. If this condition is not met, the impact on the proposed design would be to add more clock tracks to reduce the maximum time displacement from each clock track by reducing the number of associated channels. Preliminary studies however, have indicated that the maximum skew across 14 channels will be small enough so that all 14 tracks can be clocked simultaneously. Investigation (see Appendix A) performed on an IR&D transport shows a maximum edge-to-edge skew of 1 micrometer (40 microinches) and a maximum edge-to-center skew of 0.75 micrometer (30 microinches). The maximum nonlinearity relative to a straight line from edge to center of tape is given on 0.075 micrometer (3 microinches). At a maximum tape packing density of 0.8 megabit per meter (20 kilobits per inch), and with 66 tracks (sync and data) from the middle of the tape to the edge, the maximum displacement from bit to bit is:

$$\frac{0.95 \times 10^{-6} \text{ m}}{66 \text{ Tracks}} \cdot 0.8 \times 10^{6} \text{ b/m or}$$

$$9.09 \times 10^{-3} \text{ bit per track displacement.}$$

Adding another 10-percent maximum displacement for the non-linearity yields approximately 1-percent displacement from bit to bit. Allowing a factor of three for additional time-base error yields a maximum displacement of ±21 percent of a bit period from the clock track. Thus, each group of 14 data tracks can be clocked by the data clocks derived from the center data tracks.

The size of the Dejitter-Deskew Buffer must be great enough to accommodate the maximum skew experienced across the entire tape. Again, based on the above numbers, the maximum skew is determined to be:

$$1 \times 10^{-6} \text{ m} \cdot 0.8 \times 10^{6} \text{ Mb/m or}$$

0.8 bit displacement

Again using a factor of three for time-base error margin, the resultant maximum displacement is estimated at ±3 bits. To accomodate this amount, an eight-bit circulating buffer is required. The operation of the Dejitter Deskew Buffer can be visualized using the circular timing diagram shown in Figure 2-20; a block diagram of the Buffer is shown in Figure 2-21. Assume that there is a skew of three bits relative to center associated with the playback data, such that the data on track 1 leads the rest of the data. Since the skew is relative to the center clock channel that determines the readout of the buffer, three bits of data will be read into the circulating register before clock pulses arrive at the system counter through the input to the four-bit delay register (Delay 1). At the time of arrival of the seventh data bit, readout of bit 1, track 1 (and data tracks 2 through 14, since they are all clocked into the buffer synchronous with clock 1) will occur. As successive data bits are received at the buffer input, additional bits will be read out.

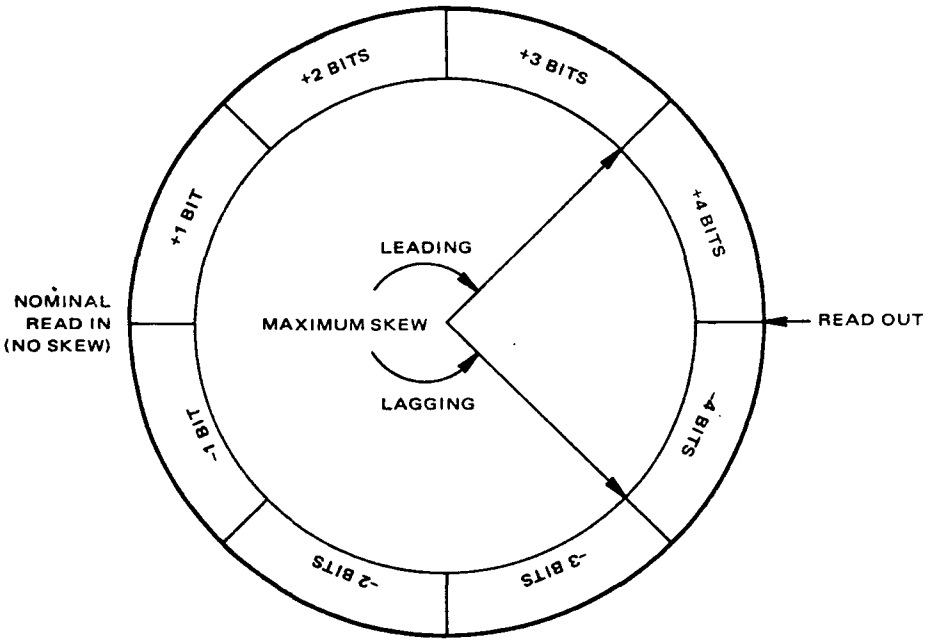


Figure 2-20. Dejitter-Deskew Buffer Circular Timing Diagram

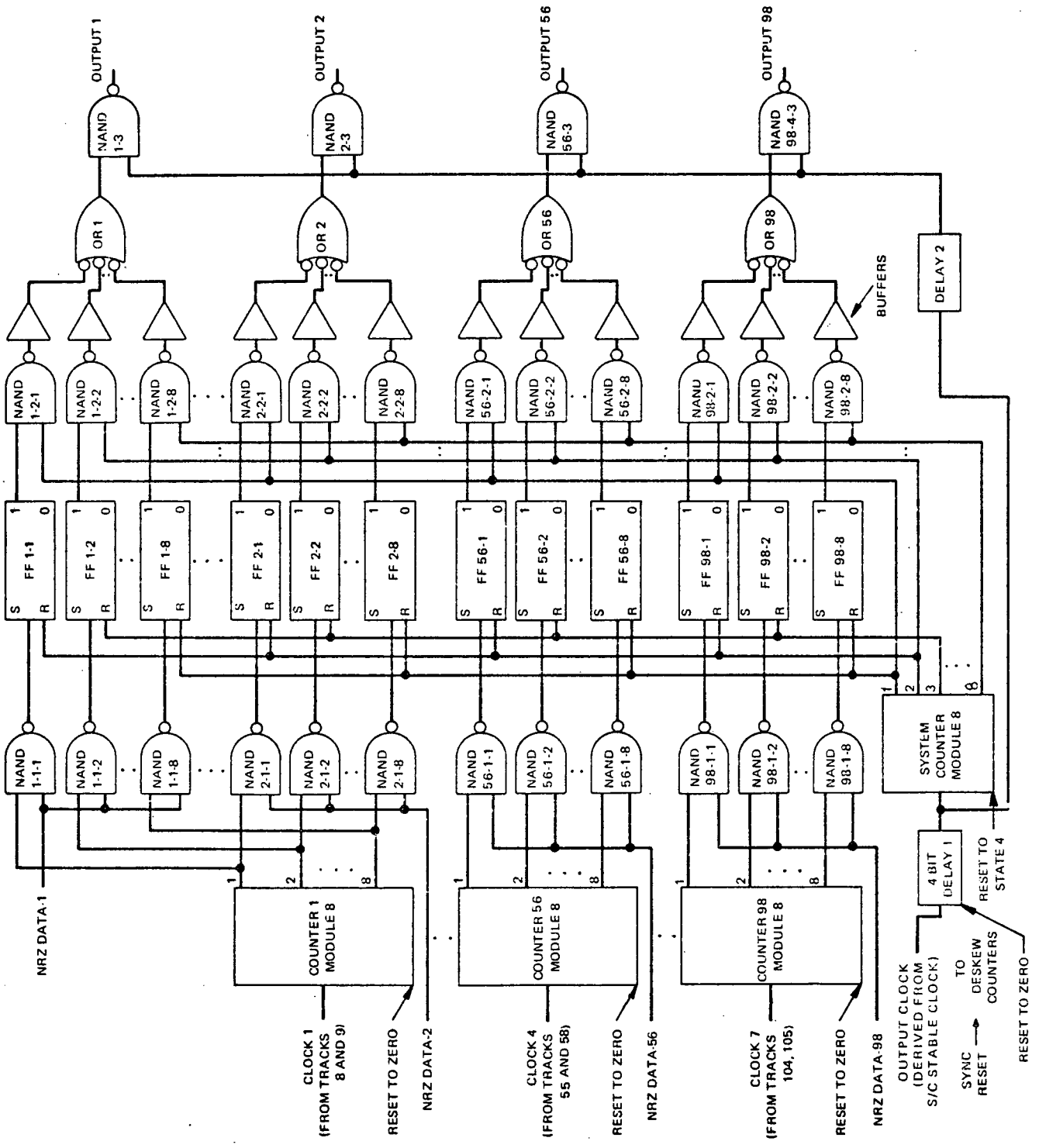


Figure 2-21. Dejitter-Deskew Buffer, Block Diagram

If the amount of skew does not change, the relative phasing between readin and readout will remain constant. Where the amount of skew does change, the relative phasing between readin and readout will also change, but the read-out rate will remain constant. Similarly, if the tape skew were such that the data on tracks 1 through 14 lagged the reference clock track by three bits, the resulting delay between read-in and read-out would be one bit, rather than the seven bits of the previous case.

Since the read-in and read-out timing is asynchronous, the skew can vary between the two limits described without affecting the data output. All that is required is that the average clock rates are the same frequency and that the maximum skew is such that the peak phase differential between any data bit and its reference clock is less than the equivalent number of bits in the Deskewing Buffer. The first condition is guaranteed by the fact that all input clocks are derived from the same tape while the second condition determines the size of the circulating register and the counting logic.

The operation of the logic shown in Figure 2-21 can be described as follows. Initially and after every 32 bits thereafter, the counters are flywheel-reset by the sync decode to the zero state except for the System Counter, which is flywheel preset to state 4 to account for the nominal four-bit delay between readin and readout. If the skew is positive, as in the first case above, clock pulse 1 of channel is first to arrive and sets the channel 1 counter logic to "1" on the trailing edge of the clock 1 pulse. This counter output is one of the inputs to AND 1-1-1; the other input is the data bit 1. When both are present at the input to the AND gate, a "1" output results. This output goes to the Set input of Flip-Flop 1-1, resulting in a "1" output. The "1" output of the flip-flop is an input to AND 1-2-1. This information bit will not proceed any

further until sufficient time has elapsed to allow the "latest" bit of the character (in data channel 98) to arrive at its corresponding position (AND 98-2-1).

Information bits 1 of channels 2 through 14 are also clocked in simulataneously with Data bit 1, track 1. The same sequence of events occurs for clock pulse 1 and data bit 1 in all the other channels.

Since we are assuming that the maximum six-bit peak-to-peak time base error is occurring, clock pulses derived from tracks 55 and 58 trail clock 1 by approximately three bits; i.e., clock pulse 1 of channels 55 and 58 occurs simultaneously with the third pulse of clock 1. It is desired that the system counter activate AND 1-2-1, AND 2-2-1, ..., AND 98-2-1 after all have received information pulse 1. Since in the maximum skew case, the first data bit of channel 98 may occur three bits after the corresponding channel 55 and 58 pulses, the system counter must be delayed by at least this amount. To provide a margin of safety, Delay 1 is shown producing a four-bit delay. System count 1 causes AND 1-2-1, AND 2-2-1, ..., AND 98-2-1 to each produce an output that activates the OR gate of the appropriate channel (OR 1, OR 2, ..., OR 98). Each OR gate output appears at the input final AND gate of the channel. (AND 1-3, AND 2-3, ..., AND 98-3). Information bit 1 for all 98 data channels will appear simultaneously at the output of AND 1-3, AND 2-3, ..., AND 98-3 when Delay 2 produces an input at each of these AND gates. Delay 2 is considerably shorter than Delay 1; it should be slightly greater than the time it takes for a pulse to pass from the input of the System Counter to the input of the final AND gate.

So far, we have explained only how the first character enters the deskewing buffer with a skew of three bits edge-to-edge and arrives at the output at a later time with all the bits of the character arriving simultaneously. However, while this procedure is in progress, subsequent information bits are being read from the tape. These must be directed to the proper storage locations; bit 2 cannot be stored in FF 1-1 because this flip-flop is storing bit 1. Correct storage is achieved in the following way. The positive edge of clock pulse 2 (which precedes information bit 2) in channel 1 will cause Counter 1 to advance to count 2. Count 2 and information bit 2 will both appear at AND 1-1-2, producing an output that sets FF1-2. This bit cannot proceed to the channel output until clock pulse 2 (derived from Tracks 55 and 58) have passed through Delay 1 and set the System Counter to count 4. By that time, all bits of character 2 have reached the second flip-flop in their respective channels (FF 1-2, FF 2-2, ..., FF 98-2). On system count 2, each proceeds through the next AND gate, then the OR gate, and finanlly appears at the output of the last AND gate. All 98 bits of character 2 arrive simultaneously at the output of the Dejitter-Deskewing Buffer, following character 1 by one bit time. One additional function performed by the System Counter is to reset to zero the flip-flops whose information has reached the output of the deskewing buffer. For example, FF 1-1, FF 2-1, ..., FF 98-1 are reset on the leading edge of system count 2.

The deskewing system described offers several advantages:

(1) The skew need not vary linearly across the tracks. Deskewing will take place properly as long as the skew from the center track to either edge does not exceed the maximum expected value, and the skew across the groups of 14 tracks are within $\pm\frac{1}{2}$ bit relative to the center clock tracks.

(2) The system will operate properly for any amount of skew up to the maximum value.

(3) The skew need not be constant with time. Correct operation will be maintained as the skew varies with time as long as it is within the expected limits.

2.1.3.9 Parallel-Serial Converter- 98/2 Digital Multiplexer

The parallel-serial converter reformats the data from one parallel 98-bit word, occurring once every 760 ns, to two serial 66.58-Mb/s data streams. The two serial data streams modulate the four-phase PM transmitter. Four-phase modulation is achieved by combining the outputs of two biphase modulators operating in quadrature. One of the serial data streams is delayed by one-half bit. This does not increase the bandwidth required, but does allow identification of the two recovered channels on the ground.

Two parallel-input, serial-output shift registers, with a relative delay of one-half bit in phasing, are used for the parallel-serial conversion. To provide the necessary time to load the registers, each of the shift registers is divided into two sections. Each section is loaded and read out alternately, thereby providing continuous output data. Timing and gating logic is provided to control the loading and readout of the two registers.

2.1.3.9.a Timing For Parallel-Serial Converter

The data rate out of the deskew buffers is at 1.318 Mb/s, which corresponds to 760 ns per bit. During this time, 98 bits are presented in parallel to the parallel-serial converter. Figure 2-22 shows the timing relationships for loading and shifting the data out of the P-S Converter shift registers. The

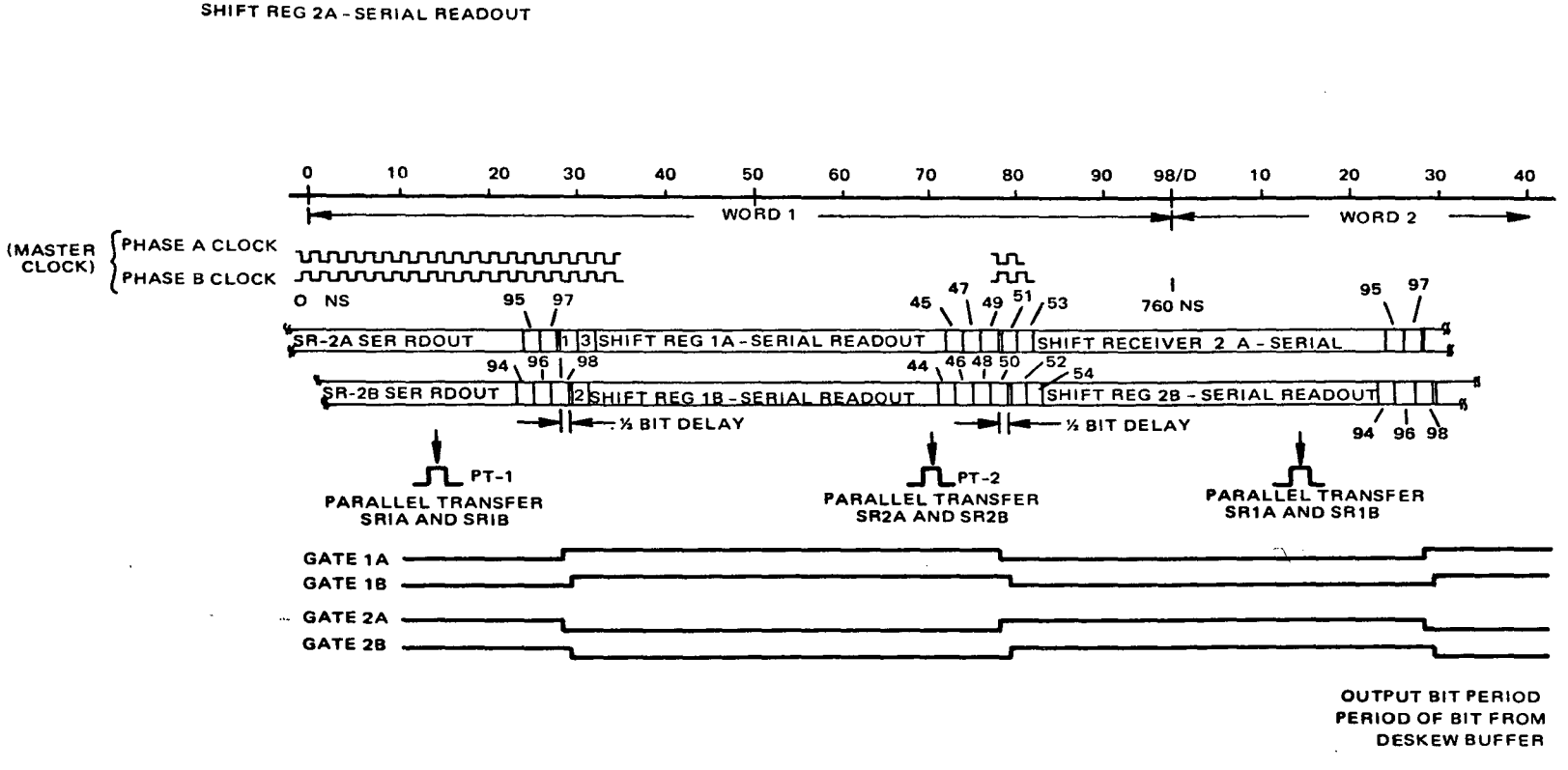


Figure 2-22. Parallel-Serial Converter Timing Diagram

time during which the 98 bits are present at the deskew register output is called word 1. This time (760 ns) is divided into 98 half-bit segments, to correspond to the two sets of 49 bits to be shifted out.

During segments 13 and 14, shift registers SR1A and SR1B are loaded with the first 50 bits of the output data, SR1A storing all the odd bits, and SR1B all the even bits. At the beginning of segment 28, the control circuitry is switched so that the phase A data output will be driven from SR1A, and phase A clock pulses are directed to SR1A. Similarly, at the beginning of segment 29, the phase B clock is directed to SR1B, and the phase B data output is driven from SR1B. The SR1A and SR1B circuitry is shown in Figure 2-23 and Figure 2-24. SR1A and SR1B will continue to shift data out at the 64.58-Mb/s rate for the next 50 segments. At the beginning of segment 69, during the above read out, shift registers SR2A and SR2B are loaded with the remaining data bits of the word. At the end of the SR1A and SR1B readouts, segments 78 and 79 respectively, control and clock are transferred to shift registers SR2A and SR2B. These registers then serially transfer out the remaining bits, 57 through 98 of the word. During this portion of the data traansfers, SR1A and SR1B are again loaded during segments 15 and 16 of the following word. The Parallel-Serial Converter thus provides a continuous transfer of serial data to the transmit circuitry from the deskew buffers.

2.1.3.9.b Control Logic for Parallel-Serial Converter

The control logic for the Converter consists of a 49-state converter with combinational logic to decode the parallel transfer and gating signals. The counter is driven from the 64.58-MHz master clock. Both the master clock phase A and its complement phase B are required to provide the proper phasing for the data outputs.

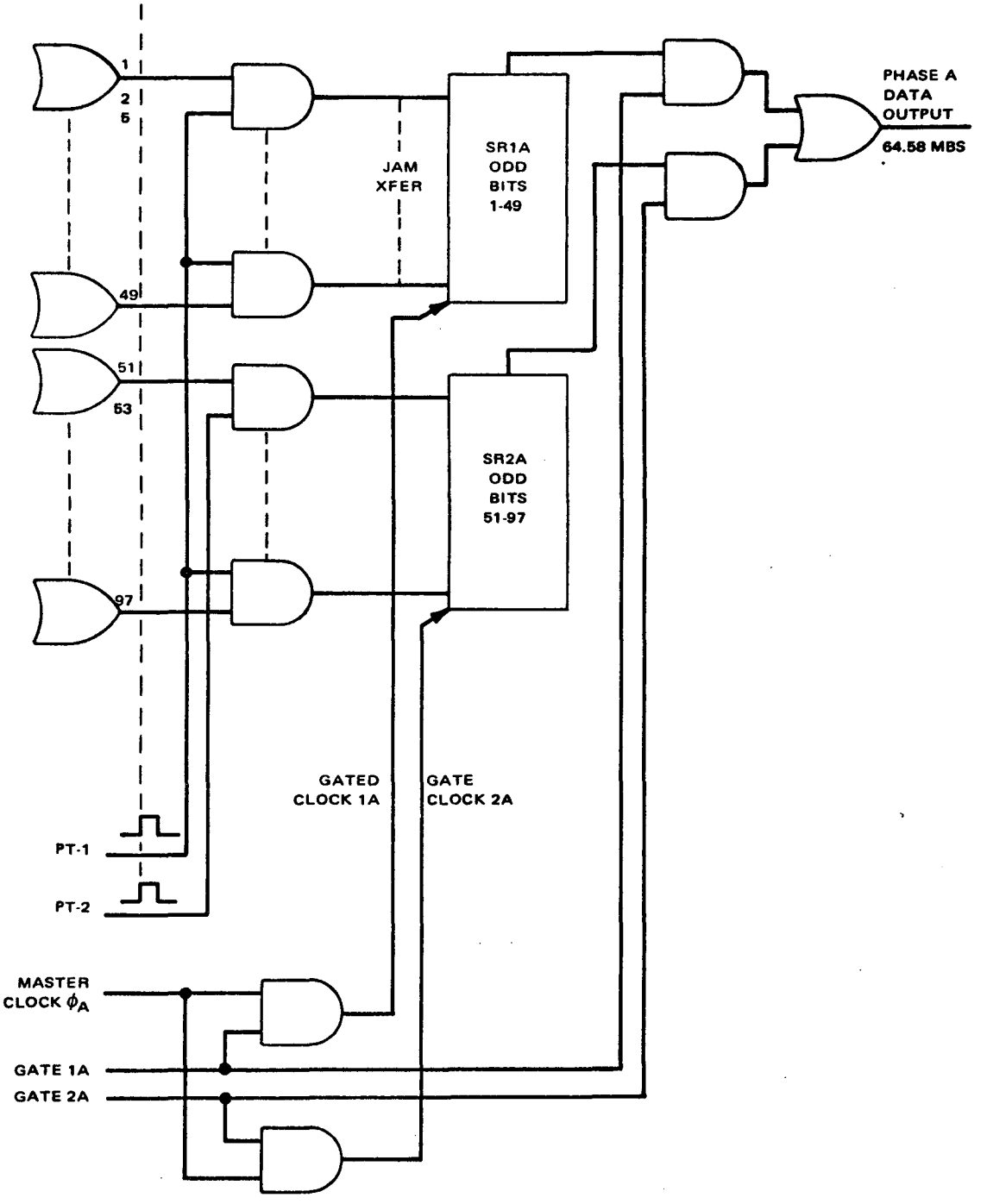


Figure 2-23. Parallel-Serial Converter; Shift Registers 1A and 1B

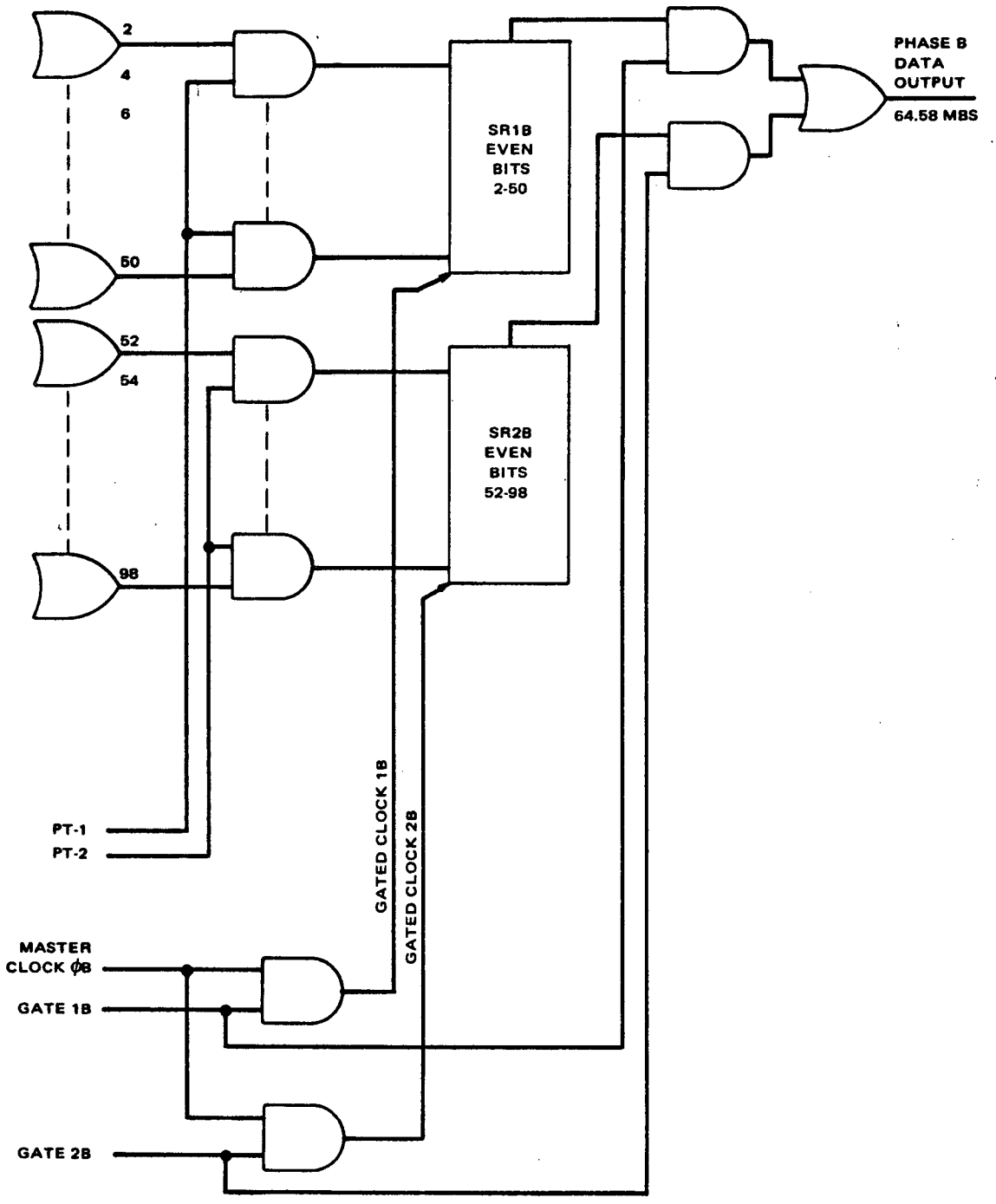


Figure 2-24. Parallel-Serial Converter; Shift Registers 2A and 2B.

The required decodes are segments 13 and 14, 28, 29, 69 and 70, 78, and 79. Figure 2-25 shows the control logic implementation. The 49-state counter is shown implemented with two seven-state Johnson counters. A smaller configuration is possible, but this arrangement was selected for estimating purposes.

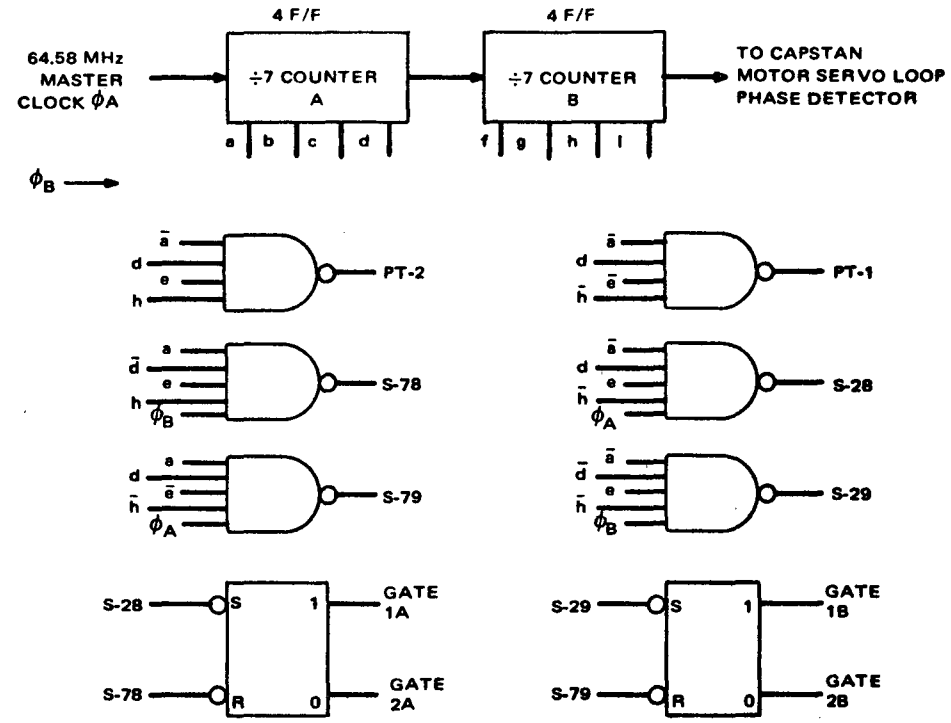
The decoding circuitry is also shown in Figure 2-25. Although the counter used is a 49-state device, the 98 segments are derived from decoding the 49 states of the counters and using the A and B clock phases.

2.1.3.9.c Implementation

The Parallel-Serial Converter is implemented with TTLS logic because of the high data rates of the output bit stream. The flip-flops used for the shift registers and the counters are the SN 54S112 type. The additional circuitry for parallel-loading the SR's and controlling the data transfers is also implemented family. Additional buffering of the clock circuits for the shift register is required; this is not shown on the logic diagrams of Figures 2-24 and 2-25. These are, however, included in the power and size estimations.

2.1.3.10 Capstan Servo-Loop Reference Signal

The speed of the playback circuitry is determined by a reference signal derived by comparing the reconstructed clock derived from the center tracks (data tracks 55 and 58) with the master system clock. The master clock frequency is 49 times that of the data rate when the system is in the playback mode. The block diagram of Figure 12 shows the 64.58-MHz master clock divided by a 49-state counter and then providing one of the inputs to a phase detector, while the reconstructed clock provides the other input. The resulting phase-difference output provides the error signals for the capstan-motor servo loop. Difference in timing between the master clock 64.58-MHz clock and the derived clock are absorbed in the Dejitter-Deskew Buffer circuit. Thus, in addition to handling time-base errors in the playback system due to jitter and tape skew, the Buffer must also be able to accommodate jitter in the tape motion.



CTR A

STATE	a	b	c	d
1	0	0	0	0
2	1	0	0	0
3	1	1	0	0
4	1	1	1	0
5	1	1	1	1
6	0	1	1	1
7	0	0	1	1

CTR B

STATE	e	f	g	h
1	0	0	0	0
2	1	0	0	0
3	1	1	0	0
4	1	1	1	0
5	1	1	1	1
6	0	1	1	1
7	0	0	1	1

SEGMENT	DECODES
14	(A - 7) (B-1) φA } PT-1
15	(A - 7) (B-1) φB } PT-1
28	(A - 7) (B-2) φB
29	(A - 1) (B-3) φA
69	(A - 7) (B - 5) φA } PT-2
70	(A - 7) (B - 5) φB } PT-2
78	(A - 4) (B-6) φB
79	(A - 5) (B-6) φA

Figure 2-25. Parallel-Serial Converter; Control Logic

2.2 Tape Transport

2.2.1 Mechanical Description

The primary tape transport configuration proposed is the co-planar, capstan-driven, negator-tension machine shown in Figure 2-26. This machine is derived from the video tape recorder developed by RCA for ERTS. The rotating head wheel and the associated angular-momentum compensating motor is not, of course, required on a longitudinal tape recorder and so is deleted. The synchronous-hysteresis motor, coupled by a belt to the drive capstan, will be changed to a servo-controlled, brushless, dc torque motor and optical encoder for commutation and speed control right on the capstan shaft, shown in Figure 2-27. This drive system will be more reliable, consume less power, have less jitter, readily allow a change in speed if required, and is more suited to servo control of the output-data rate. It is a development of the capstan drive used on the Scanning Radiometer Tape Recorders used on the ITOS space-craft. We propose to retain the pressure rollers on the tape reels, which, on the ERTS video tape recorder, ensure excellent tape stacking and tracking. Because the length of 0.03 mm (0.0012 in.) thick by 50.8-mm (2 in.) wide magnetic tape is increased to 1040 m (3400 ft.), some changes will be necessary in the negator tape tensioning system. In order to keep the number of negator turns within practical bounds, the gear ratio between the negator system and the tape reels will be increased. A non-contacting, dc powered, erase head, of a type used previously by AED on a classified program, will be used to restore the tape to a zero-remanance condition on all tracks before recording a new set of data. The single, multi-track, read-write magnetic head will be of the ultra-hard mono-bloc type. RCA has developed

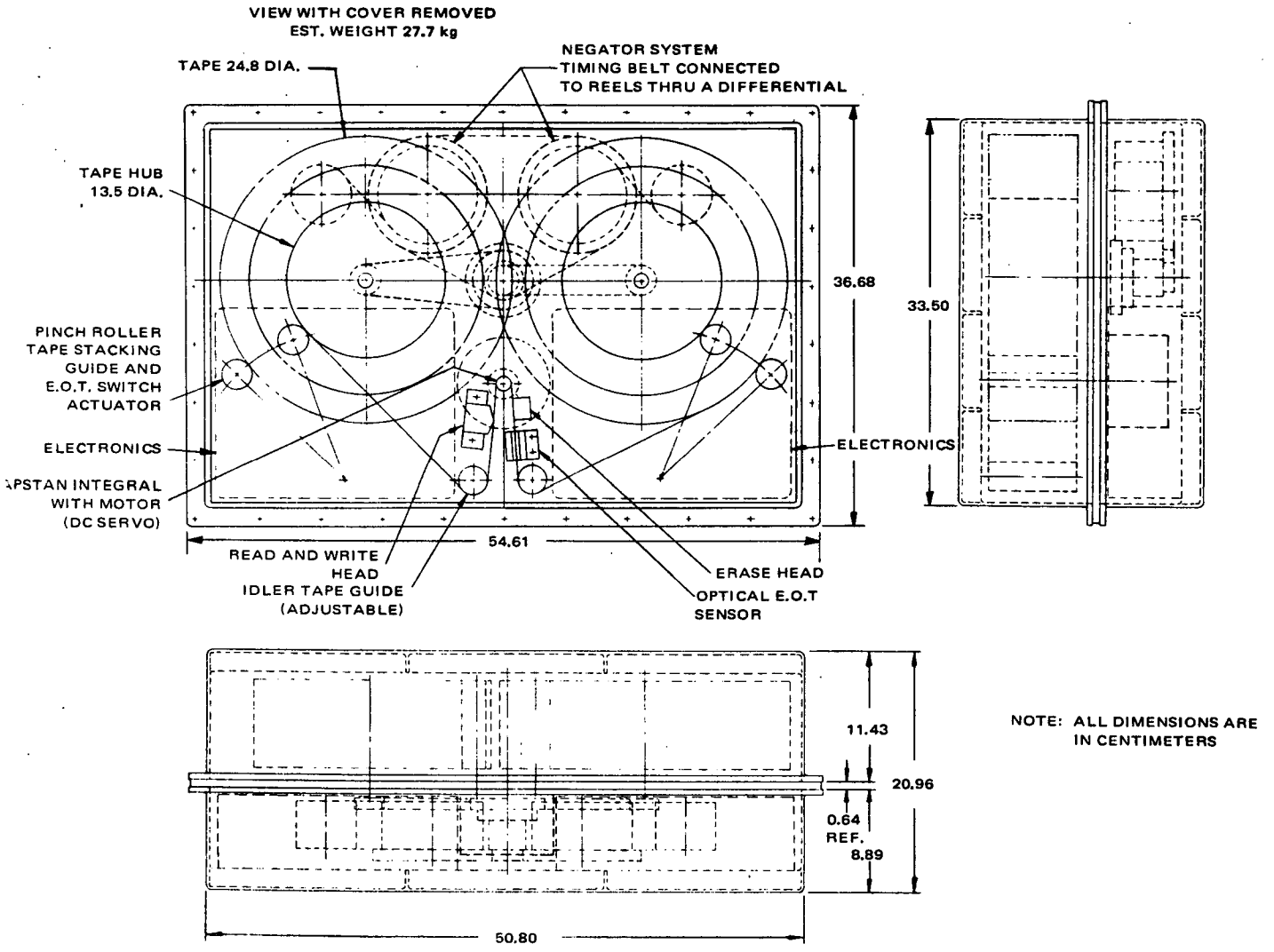


Figure 2-26. Primary Tape Transport Configuration

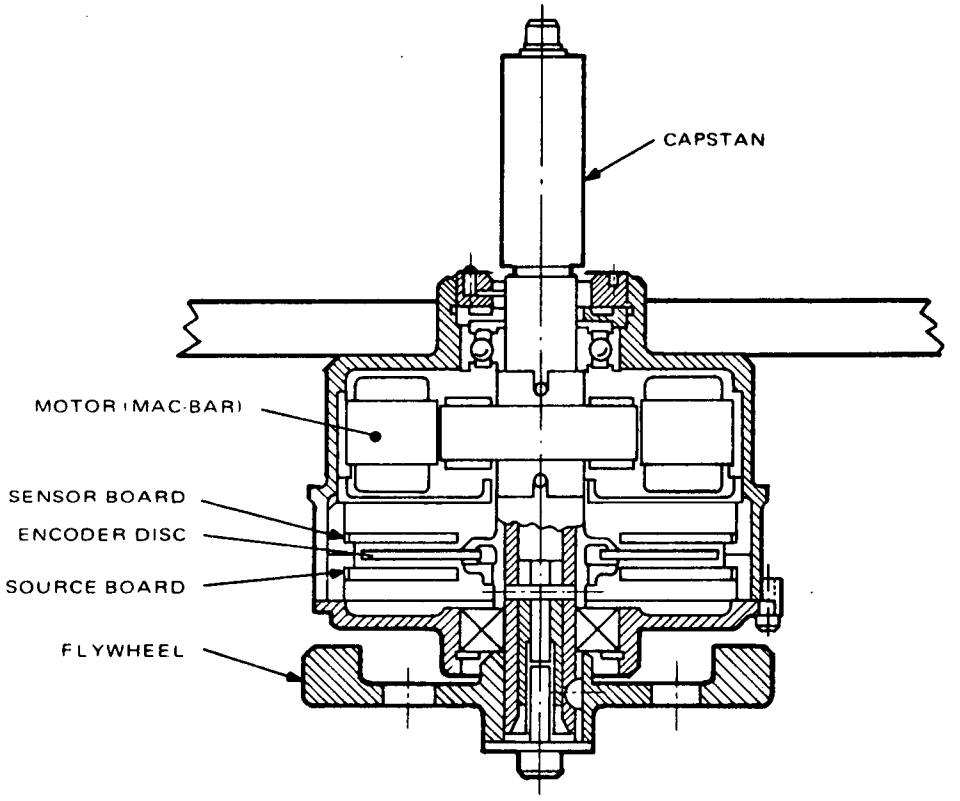


Figure 2-27. Torque Motor With Optical Encoder

the techniques for fabricating long-life, high-density, multi-track magnetic heads from a block of Alfecon II or ferrite on an IR&D program. The magnetic head proposed for the MCTR will be made in four blocks each having 28 tracks. Track spacing will be about 0.5 mm (0.0197 in.) the track width 0.3 mm (0.0118 in.) and the gap 0.9 μm (0.0354 in.). Single turns will couple each magnetic head to miniature toroidal ferrite transformers with multiple output turns. Following the practice on the Nimbus HDRSS, ITOS, and other spacecraft tape recorders the primary end of tape sensing will be electro-optical, using gallium arsenide light-emitting diodes, phototransistors, and sections of the magnetic tape cleared of the magnetic oxide and binder in special patterns to avoid ambiguity. Also midly abrasive deposits on the surface of the tape at the record end are proposed for the purpose of removing any debris or wear products at the magnetic-head-to-tape interface that might otherwise cause separation of the magnetic head and tape which would result in severe loss of playback signal. All bearings will be lubricated by ESSO Andok C grease and the recorder will operate in a dry CO_2-0_2 atmospheric environment, which minimizes wear at the magnetic-head-to-tape interface.

As an alternate, it is proposed to eliminate the negator tape-tensioning system with its springs, gears, belts, and bearings and the drive capstan. In this configuration, shown in Figure 2-28, there will be two brushless, dc torque motors, one integral with each reel assembly. One of these motors will be servo controlled, to pull the magnetic tape at the correct speed, while the other applies a torque (opposing the tape motion) adjusted to keep the tape at the correct tension. Tape speed in record would be sensed by an optical encoder mounted on one of the tape idlers. This system offers the potential of very high reliability, by virtue of its extreme mechanical simplicity. The reason for proposing it as an alternate instead of the primary configuration is that the concept, as applied to space-

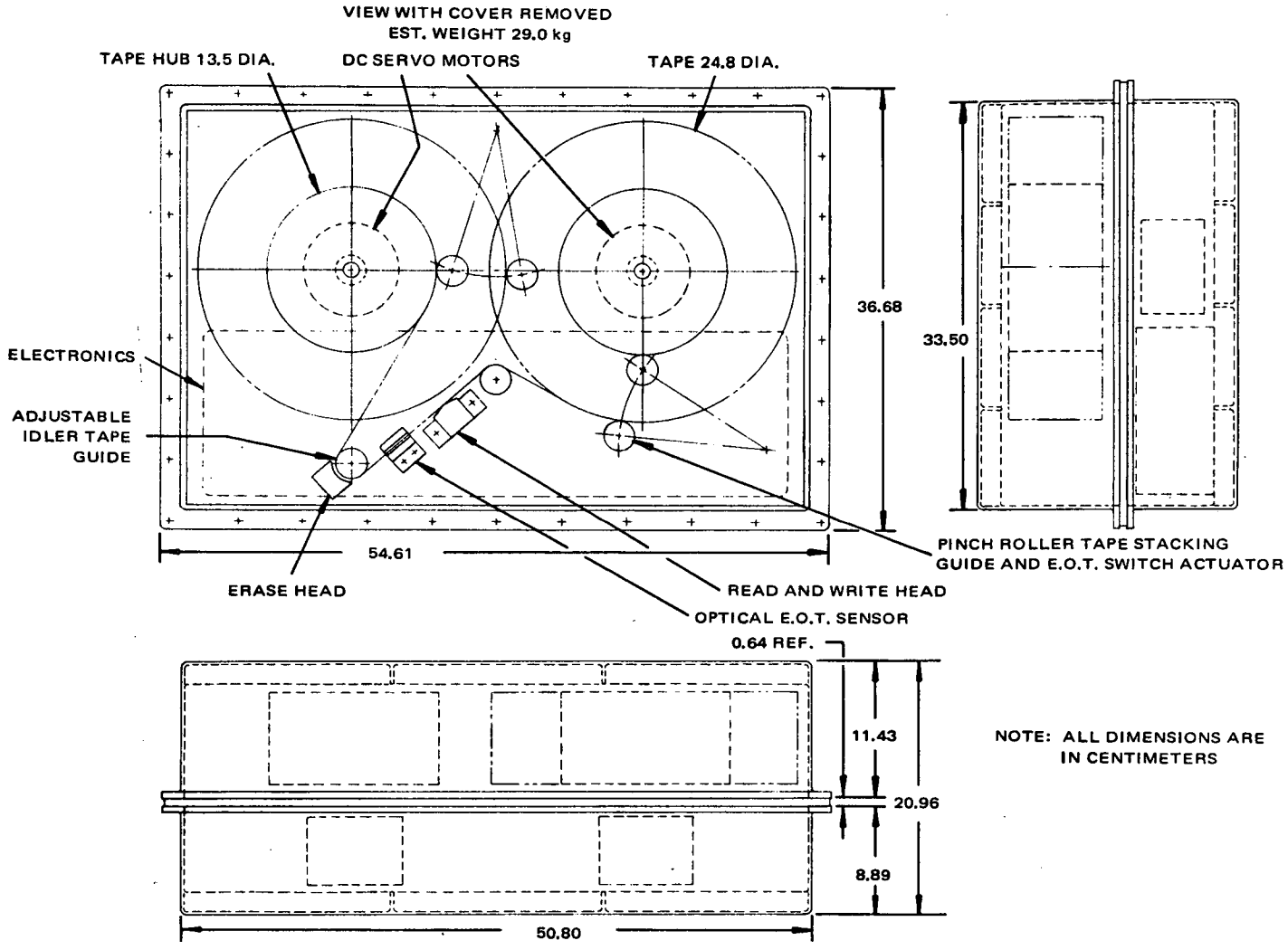


Figure 2-28. Alternate Tape Transport Configuration

craft tape recorders, is quite new and the techniques for electronically controlling the machine are still being developed. Work on this concept is in progress at AED, JPL, and elsewhere.

In the sections that follow, emphasis is placed on the primary tape transport, but wherever our studies have been extended to cover the alternate tape transport, the results are given separately.

2.2.1.1 Drive Motor Torques and Speeds

2.2.1.1.a Capstan Driven Primary Tape Transport

For the primary tape transport we have selected a brushless dc torque motor mounted integrally on the capstan shaft. A dc torque motor with commutator and brushes was rejected because of commutation problems and limited brush life. A two-speed, ac, synchronous-hysteresis motor, coupled to the capstan by a belt was rejected because of (1) servo control required during playback, which is more difficult than with a dc motor; (2) lubrication problems and life limitations using small bearings operating at high speed; (3) unreliability and life limitations of belts (4) problem of coping with belt resilience inside the servo loop; (5) low electrical efficiency especially at the lower speed; (6) start-run circuit complications; (7) synchronous hunt; (8) lower torque margins.

MacBar Inc. had developed for AED in 1968 an eight-pole, brushless, dc torque motor with six bifilar windings and built two engineering models. They had also developed a similar motor, which we are now qualifying as part of the VHRR radiometer for ITOS D and E. We have designed and built circuits for the control of this motor, including integrated-CMOS-logic chips for commutation, reversal, and phase detection. One of the engineering-model motors and breadboard drive and control circuits has been on an experimental, coaxial-reel, tape recorder carrying

460m of 50.8-mm-wide tape with more than ample torque and speed reserves. We have selected this motor for the primary tape transport.

Figure 2-29 shows the torque vs. speed characteristic of the motor. Figure 2-30 shows the motor loads for the selected capstan diameter at various tape displacements. Table 2-1A shows how this motor would behave at the high-speed playback or rewind speed for a variety of capstan diameters. The operating points are plotted on Figure 2-29; a 15-mm capstan diameter was selected because this combines a torque margin of almost 4:1, an efficiency of 82.5 percent, and modest tape-bending stessses.

2.2.1.1.b Reel Driven Alternate Tape Transport

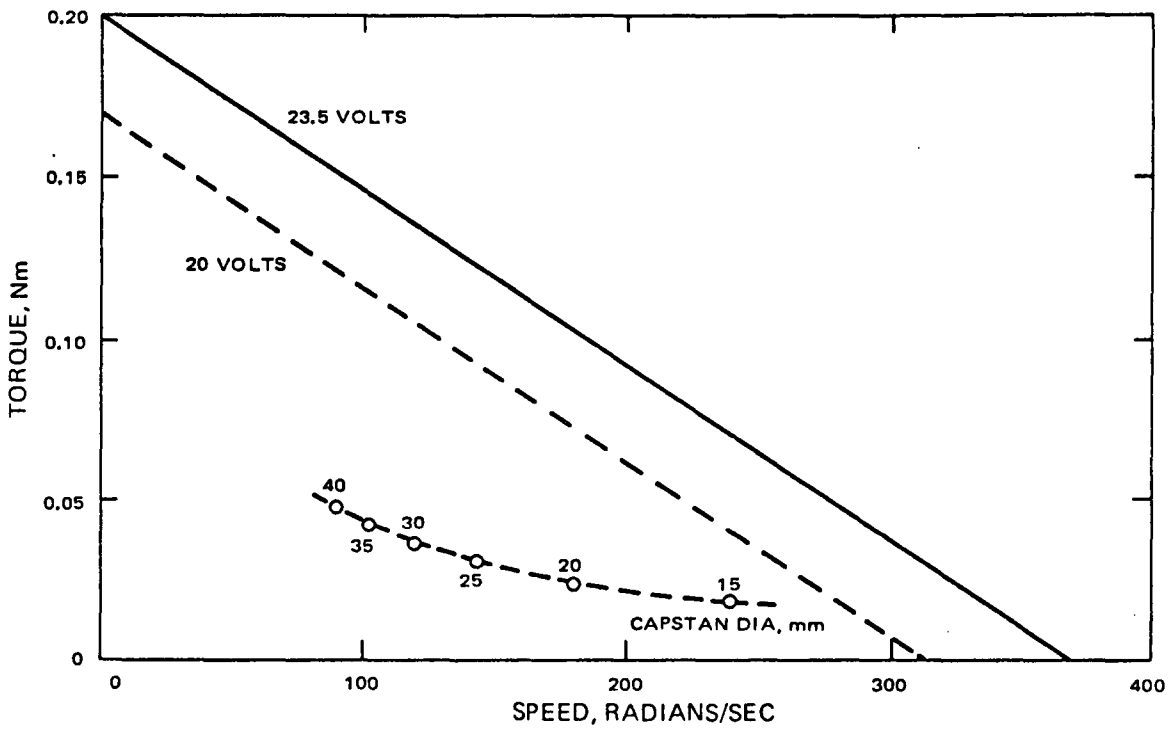
This configuration calls for two motors, each capable of delivering about the same power as the capstan motor, but at about ten times the torque level and one-tenth of the speed. Motors for this configuration will therefore have many times the number of turns and may, with advantage, have more poles and greater length or diameter.

We are proposing a motor having the torque vs. speed characteristic shown in Figure 2-31. Table 2-2 shows the operating parameters of the motors at start, middle, and end of tape for the two cases of constant restraining tape tension and constant restraining torque. The first is clearly more efficient so we have plotted these operating points on the figure showing a torque margin of over 2.5:1 on the empty reel.

TABLE 2-1A. MOTOR BEHAVIOR FOR VARIOUS CAPSTAN DIAMETERS; PRIMARY TRANSPORT

CHARACTERISTIC	VALUE					
Capstan dia, mm	15	20	25	30	35	40
Capstan torque, Nm	0.018	0.024	0.030	0.036	0.042	0.048
Current A	0.280	0.374	0.467	0.541	0.654	0.748
Capstan speed, read,rad/sec	240	180	144	120	103	90
write,rad/sec	80	60	48	40	34.4	30
Back emf, read, V	15.4	11.4	9.15	7.52	6.54	5.72
write, V	5.08	3.82	3.05	2.54	2.19	1.91
IR drop	2.10	2.80	3.50	4.06	4.91	5.62
Total voltage, read, V	17.50	14.20	12.65	11.58	11.45	11.34
write, V	7.18	6.62	6.55	6.60	7.10	7.53
Mechanical power, read, W	4.32	4.32	4.32	4.32	4.32	4.32
write, W	1.44	1.44	1.44	1.44	1.44	1.44
Electrical power read, W	4.89	5.45	5.88	6.26	7.48	8.49
to motor write, W	2.01	2.54	3.05	3.57	4.64	5.65
η (motor), read, %	88.0	70.0	73.3	68.8	57.6	50.8
write, %	69.5	56.7	47.3	40.4	31.7	25.5
Current @ 23V read, A	.218	.237	.255	.273	.326	.370
(24.5V - V_{CE}) write, W	.0875	.111	.133	.156	.202	.246
Total electrical power,read,W	5.22	5.80	6.24	6.68	7.98	9.05
write, W	2.14	2.72	3.26	3.82	4.94	5.97
η @ 24.5V read, %	82.5	74.4	69.2	64.5	54.1	47.7
η @ 24.5V write, %	67.5	53.0	44.3	37.8	29.2	24.1

NOTES: Negator System - differential tension 2.4N Tape speed 1.8 m/s read, 0.6 m/s write
For 15mm capstan and allowing 33% margin — read 283mA, write 116mA



NOTES:

8 POLES, 6 BIFILAR WINDINGS
K_v = 63.5 mV/RAD/S
K_T = 0.0642 Nm/A
R = 7.5 Ω

Figure 2-29. MCTR Drive Motor for Capstan Driven Primary Tape Transport; Torque vs. Speed.

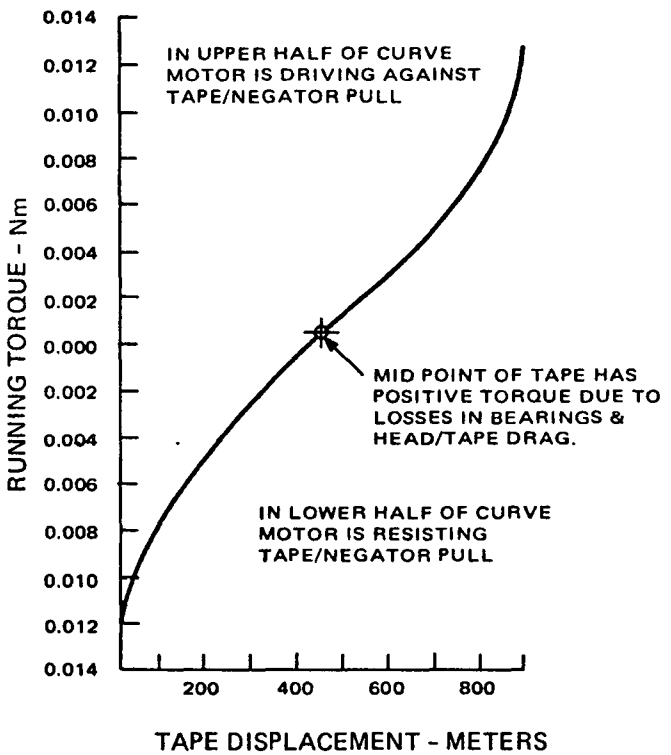


Figure 2-30. Motor Load vs. Tape Displacement; Primary Transport.

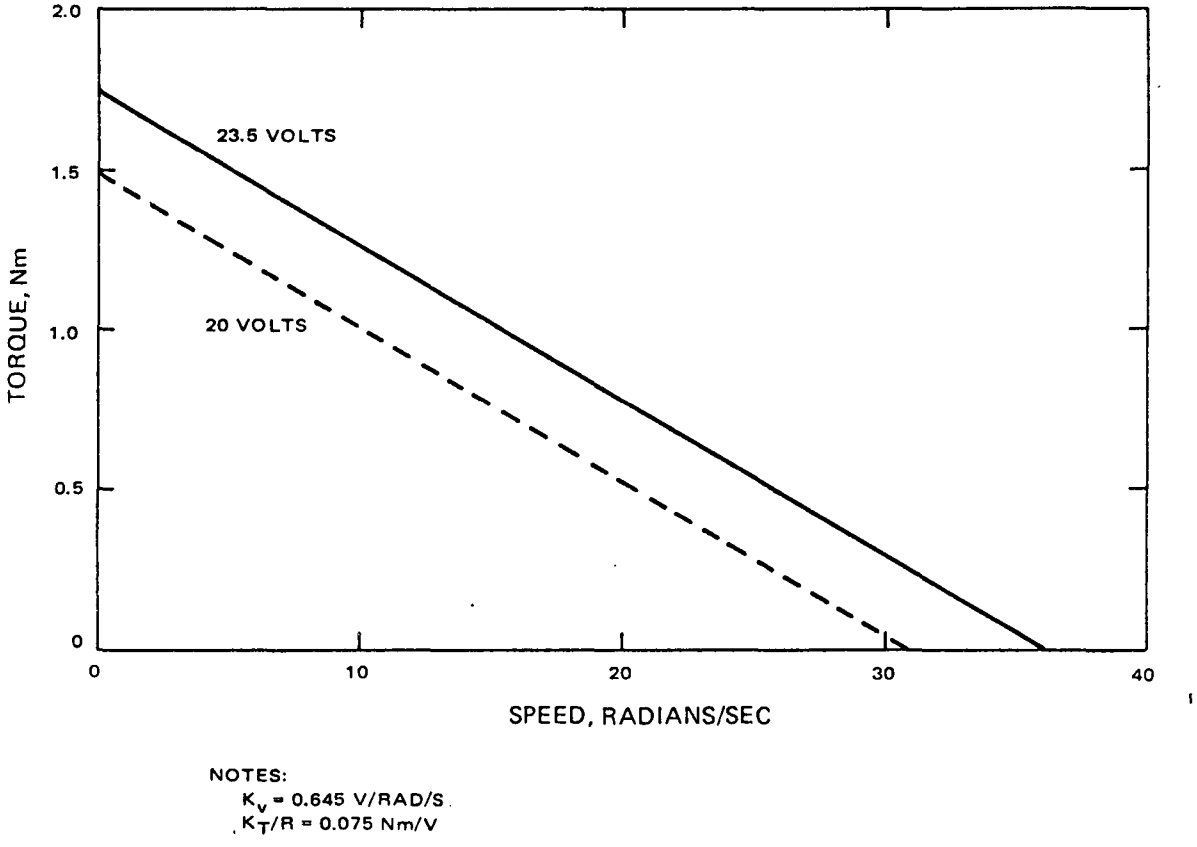


Figure 2-31. MCTR Drive Motor for Reel Driven Alternate Tape Transport; Torque vs. Speed

TABLE 2-2. MOTOR OPERATING PARAMETERS; ALTERNATE TRANSPORT

CHARACTERISTIC	VALUE		
	R_1	R_m	R_o
Radius mm	67.5	99.0	123.8
Torque (constant tension Nm	0.171	0.251	0.314
Speed Rad/sec	26.6	18.2	14.5
Power for tension watts	4.56	4.56	4.56
Torque (constant) Nm	0.314	0.314	0.314
Tension (constant torque) N	4.65	3.17	2.54
Power for tension, watts	8.33	5.70	4.56
Total power (constant tension)W	9.12	9.12	9.12
Total power (constant torque)W	12.89	11.40	12.89

NOTES: 1. Tape tension 2.54N; Speed 1.8 m/sec.
2. c.f. power for negator system 2.54N minimum tension.

2.2.1.2 Torque Margins

2.2.1.2.a Primary Tape Transport Specifications

Playback Speed at 25°C

At 23.5 volts to motor	350%
At 20.0 volts to motor	180%

Playback Speed at -10°C

At 23.5 volts to motor	245%
At 20.0 volts to motor	115%

Record Speed at 25°C

At 23.5 volts to motor	1000%
At 20.0 volts to motor	880%

Record Speed at -10°C

At 23.5 volts to motor	740%
At 20.0 volts to motor	570%

See Figure 2-30 for motor load versus tape displacement on the Primary Transport.

2.2.1.2.b Alternate Tape Transport Specifications

Playback Speed at 25°C

At 23.5 volts to motor	170%
At 20.0 volts to motor (motor not designed for low voltage)	

Playback Speed at -10°C

At 23.5 volts to motor	110%
At 20.0 volts to motor (motor not designed for low voltage)	

Record Speed at 25°C

At 23.5 volts to motor	680%

Record Speed at -10°C

At 23.5 volts to motor	500%

2.2.1.3 Tape Tensioning System

2.2.1.3.a Primary Tape Transport

Proper tensioning of the tape is by means of the well qualified "Negator" spring system. Due to the large length of tape, coupled with the considerable difference in reel diameters between the empty and full reels, the number of differential reel turns becomes rather large. For practical reasons of size and weight, the spring force is supplied by two springs operating through a gear differential and a "timing", or cogged belt, reducing drive from the reels. The ratio from reels to springs is approximately six to one.

Neither the gear differential nor the timing-belt drive are new to recorder design. The differential is rather common in application and the "timing" belt drive is used on the ERTS recorder.

In detail, each reel is connected to the differential by a timing belt, and a two-to-one reduction in effective negator turns is obtained at this level. The output gear of the differential is connected by means of another timing belt to each of the two negator power drums in such a manner that a three-to-one reduction is effected for a total reduction of six-to-one from reels to power drums.

The Negator springs selected in this preliminary design phase are of Havar material, with a projected minimum fatigue life of at least 30,000 cycles. At four spring cycles for each record and playback sequence, and 16 ninety-minute orbits per day, the total number of cycles per year would be 23,400. There is an adequate margin including testing time.

See Figure 2-32 for a curve of the tape tension versus tape displacement.

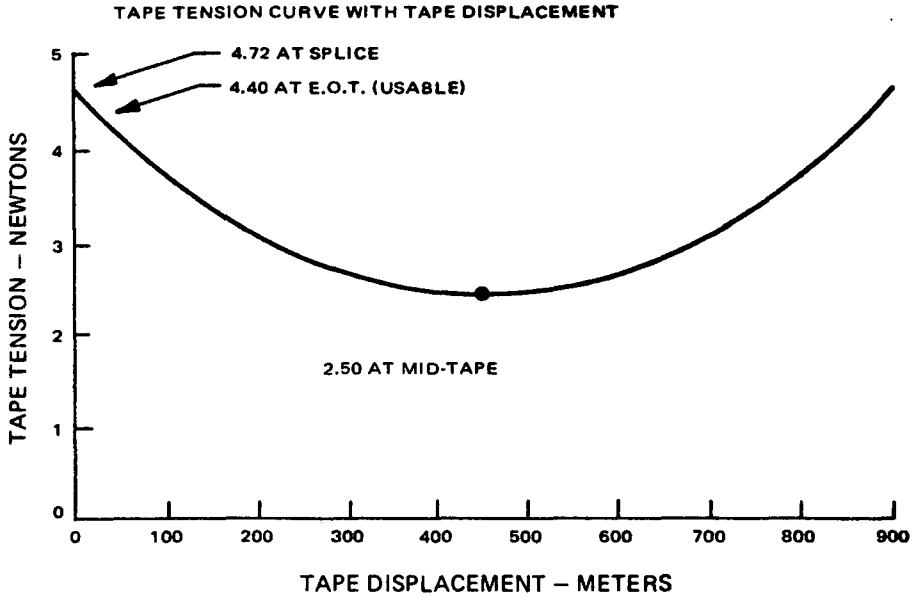


Figure 2-32. Primary Tape Transport; Tape Tension

2.2.1.3.b Alternate Tape Transport

As discussed in Paragraph 2.2.1, the alternate configuration of tape transport would eliminate the complexities of the tape tensioning system by means of adjustment of one of the torque motors to keep the tape at the correct tension.

2.2.1.4 Tape Tracking

2.2.1.4.a Primary Tape Transport

In the coplanar reel arrangement selected for the recorder, the magnetic tape will be passed from reel to reel in a single plane. As shown in Figure 2-26, the capstan will be located in a central position with respect to the reels. Two idlers will be used to keep the tape properly aligned to the heads, capstan and optical end of tape sensors.

A pinch roller type of tape-stacking guide will be in spring-loaded contact with each reel at or near the point of tangency as the tape moves onto (and off) the respective reel. These rollers are used to prevent the trapping of air under the stacking tape, especially at high speeds. This will ensure extremely tight, smooth stacking of the tape, a definite advantage in tracking control and resistance to transverse movement of the tape on its reel during both normal recorder operation and environmental exposure.

Precise tape tracking in the head-capstan area will be accomplished by making the two idlers adjustable in vertical relationship to the plane of the chassis mounting surface. Test results on a similar recorder at RCA have shown that tracking variations are compatible with the head-track spacing considered for the recorder.

No edge guiding is considered and the tests referred to have revealed no adverse affects on tracking due to one-g conditions.

2.2.1.4.b Alternate Tape Transport

Tape tracking on this transport would be essentially the same as for the primary transport. The two idlers flanking the head and optical end-of-tape area would be vertically

adjustable with respect to the mounting surface and the same pinch roller tape stacking guides would be used as shown in Figure 2-27.

2.2.1.5 Angular Momentum

At the start of playback, most of the tape is on the take-up reel and at the end it is all on the supply reel. At mid-tape, both reels are running at the same velocity and have the same inertia, but at any other time this is not so. In consequence, the angular momentum of the system varies continuously from the start of playback to the end.

The variation in angular momentum was studied for two cases: co-rotating reels and contra-rotating reels. The first case represents the primary tape transport, whose angular momentum may be balanced at two tape positions by selecting the appropriate size of the flywheel on the capstan shaft, which rotates faster than the reels and in the opposite direction. The residual angular momentum is shown on curve 1 of Figure 2-33. The peak value is 0.02 kgm^2/s (0.0148 lb ft s). A 0.86-kg (1.9-lb) capstan flywheel is required to achieve this.

The second case represents the alternate tape transport whose angular momentum may be balanced at three tape positions by selecting the right empty reel inertias. The residual angular momentum is shown on curve of Figure 2-33. The peak value is 0.018 kgm^2/s (0.0133 lb ft s). The weight of the empty reels must be increased to 3.3 kg (7.3 lb) to achieve this.

For the quantity of tape and tape speeds we need, we can reduce the unbalanced angular momentum by reducing the ratio of full-to-empty reel radii ($n = R_o/R_1$) and increasing R_o. However, the price is an increase in plan area of the tape transport.

The uncompensated angular momentum formula shown in Figure 2-34 has been enumerated over the range $n = 1.2$ to 2.0, $k = 0.5$ to 1.0, and $c = 0$ to 0.5 for case 1 and 0 to 1.05 for case 2. A computer-generated tabulation of the result forms Appendix B. These numbers are applicable to tape recorders of all types and sizes and are, therefore, of general interest.

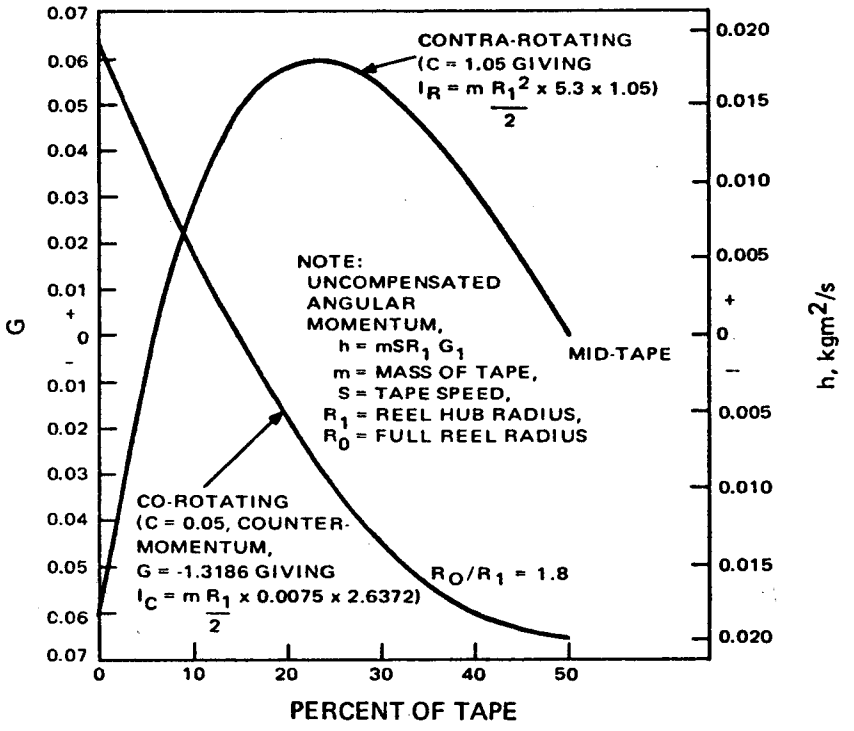


Figure 2-33. Angular Momentum of Tape Reels vs. Percentage of Tape on Reel

DERIVATION

UNCOMPENSATED ANGULAR MOMENTUM, h.

$$h = mS\frac{R_1}{2}\left\{\frac{C(n^2+1)/(n-1) + (n^2-1)(1-k)^2 + 2(1-k)}{\left[(n^2-1)(1-k)+1\right]^{1/2}}\right.$$

CO-ROTATION ↘

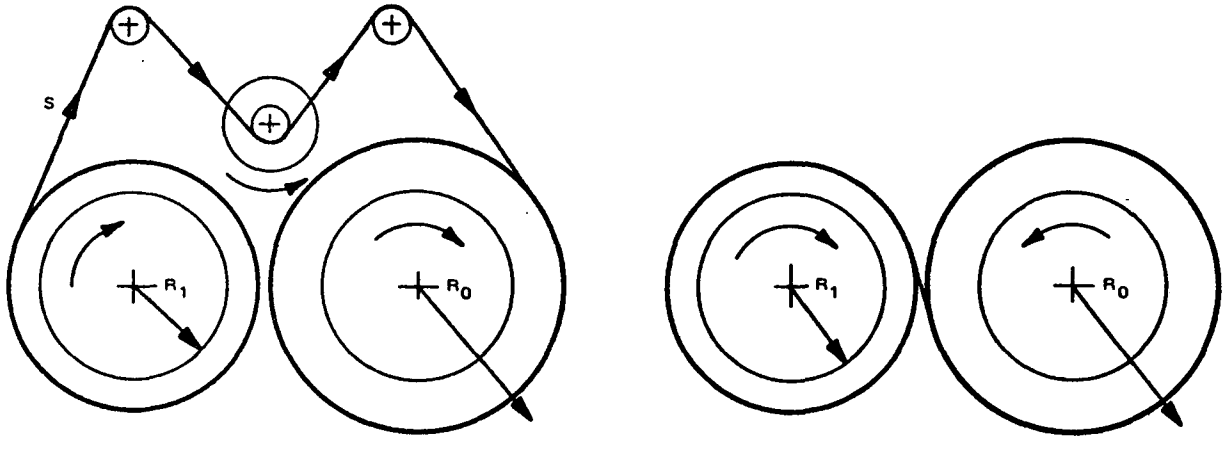
$$\left. \pm \frac{C(n^2+1)/(n-1) + (n^2-1)k^2 + 2k}{\left[(n^2-1)k+1\right]^{1/2}}\right\}$$

↗ CONTRA-ROTATION

WHERE $C = 1$ for $h = 0$ at $k = 0$ and $k = 1$ (CONTRA-ROTATION)

$n = R_0/R_1$, S = TAPE SPEED, l = TAPE LENGTH, m = TAPE MASS

k = TAPE USAGE $= \frac{St}{l}$ $(1>k>0)$



CASE 1
CO-ROTATION

CASE 2
CONTRA-ROTATION

IN OUR CASE m = 2.6 Kg, S = 1.72 m/s, R_1 = 67.5 mm, N = 1.8

Figure 2-34. Derivation of Angular Momentum Formula

2.2.1.6 Mechanical Stressing

The coplanar, or side by side arrangement of the reels on an essentially flat chassis plate should present no unusual stress loading or distortion problems. All dynamic moments are minimal, since all high inertia elements are mounted very closely to either the upper- or under-side of the chassis plate.

Obviously, a coplanar transport of this configuration could be adversely affected by distortion of the pressurized enclosure or misalignment of the spacecraft mounting surfaces. In the former case, the enclosure will be designed and strengthened against this possibility. The interface with the spacecraft can be controlled by suitable machining and/or shimming procedures.

2.2.1.7 Lubrication

The use of Esso Andok C grease in the bearings of the recorders on several other programs has been so successful that this grease becomes the first choice as a lubricant. It solves the problems of lubricant migration and rapid oxidation associated with some oils.

Obviously, if many bearings are used in the transport assembly, the greater torque required from the use of grease (especially at low temperature) could be troublesome. The MCTR configuration, with the integral capstan and motor shaft, limits the number of bearings to the absolute minimum consistent with precision tape handling and tracking.

Correspondence with the manufacturer of the Andok C grease is included as Appendix C.

2.2.1.8 Gas Environment

The IITRI (Illinois Institute of Technology Research Institute) report has recommended a controlled relative humidity (RH) for the atmosphere maintained in the pressure can of the tape transport. A life test is currently in process, using the IITRI recommended RH with 3M551 tape and heads with Alfesil pole tips. The atmosphere is approximately 80 percent air, 16 percent

N and 4 percent He, a mixture which has been working well on an existing program.

As a result of a head tape stiction study program performed at RCA, tests have been made with a recorder operating in an environment of 80 percent CO_2 and 20 percent O_2, coupled with extremely low relative humidity. These tests have shown significant improvement in noise levels with no tape damage or stiction at temperatures up to 65° C.

A recent test has clearly indicated that extremely low tape frictional drag and greatly extended head-tape life can be realized at a typical tape recorder operating temperature of $+25^{\circ}$C, over a prolonged period of time, through the use of CO_2 and O_2 with a low moisture content and by periodic head cleaning. The head cleaning is accomplished by use of a chromic oxide coating on the tape outside the normal working area, but accessible when desired. Head wear was minimal and the mechanical components show no deleterious effects due to the CO_2-O_2 atmosphere.

2.2.1.9 Enclosure Design

2.2.1.9.a Primary Tape Transport

The transport enclosure will be composed of two pieces: (1) a base, which will contain the tape transport and all electronics, and (2) a pressure-tight cover. Both the cover and base will be machined from forged ZK60A-T5 magnesium to ensure both adequate strength with minimum weight, and to eliminate any possibility of a porous and therefore leaky housing.

The enclosure will be hermetically sealed by an "O" ring and machined surfaces bolted together. The size and weight are as shown in Figure 2-26.

2.2.1.9.b Alternate Tape Transport

This enclosure will be almost identical with that for the primary tape transport, differing only in the packaging and location of the electronics within the base.

C7

2.2.2 Command and Control

2.2.2.1 Block Diagram and Control Logic

A block diagram of the motor drive and control system is shown in Figure 2-35. An 11-kHz clock signal is recorded and at the same time compared in a phase detector with an 11-kHz signal from the encoder velocity track (902 lines). During low-speed (0.575 m/s) playback, the previously recorded 11-kHz signal is compared with the 11-kHz clock directly. For high-speed (1.73 m/s) playback, the recorded signal is divided by a factor of 3:1, which signal the servo control loop maintains at 11 kHz at the summing point by increasing speed by a factor of 3:1.

Gain adjustment can be provided in the loop-compensation block to maintain adequate bandwidth and servo-loop phase-gain margin as required during record and playback modes.

2.2.2.2 End-of-Tape Sensing

A system for optically sensing the end of tape in both playback and record directions has been studied and a circuit derived as shown in Figure 2-36. The scheme consists of a light source (gallium arsenide, infrared, solid-state lamp) and a photo transistor, amplifier-detector combination feeding logic circuitry to control the motor On or Off.

As the opaque or read-write section of the tape is passing between the light source and detector, phototransistor Q1 remains Off, keeping Q2 Off. This allows the inverting input of Z1 to be at -24V, while the non-inverting side is held at -10V. The output of Z1 is close to 0V, thereby keeping Q3 On and -5V (logic "0") appears at the collector of Q3. When the clear end of the tape portion passes, the light into Q1 biases that stage on, which in turn drives Q2 On and switches the output of Z1 to -10V. Q3 is therefore biased Off and 0V (logic "1") appears at the output. Capacitor C1 provides sufficient switching delay to prevent a hole in the tape from inadvertently switching the motor off.

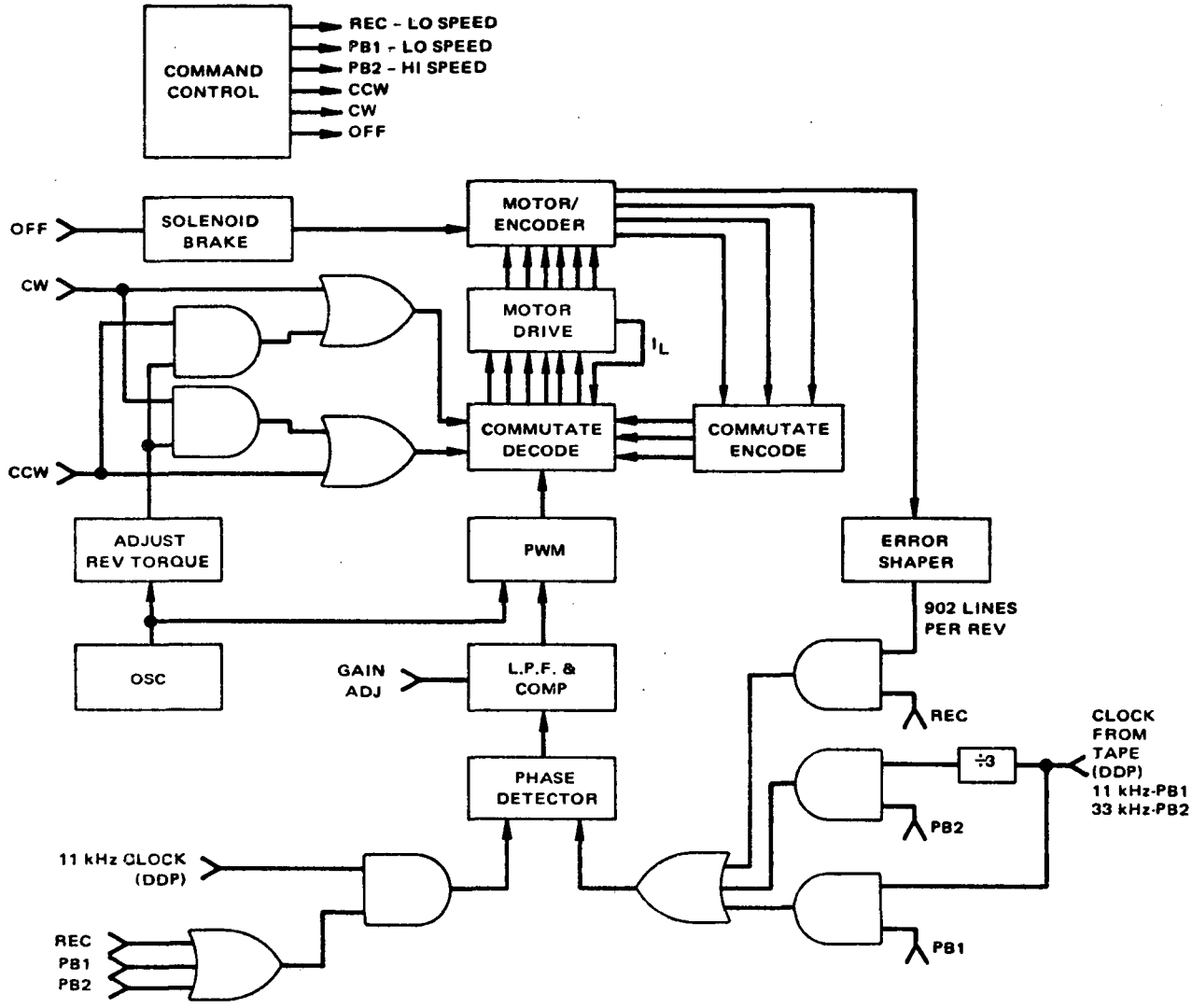


Figure 2-35. Block Diagram, MCTR Transport Motor Drive

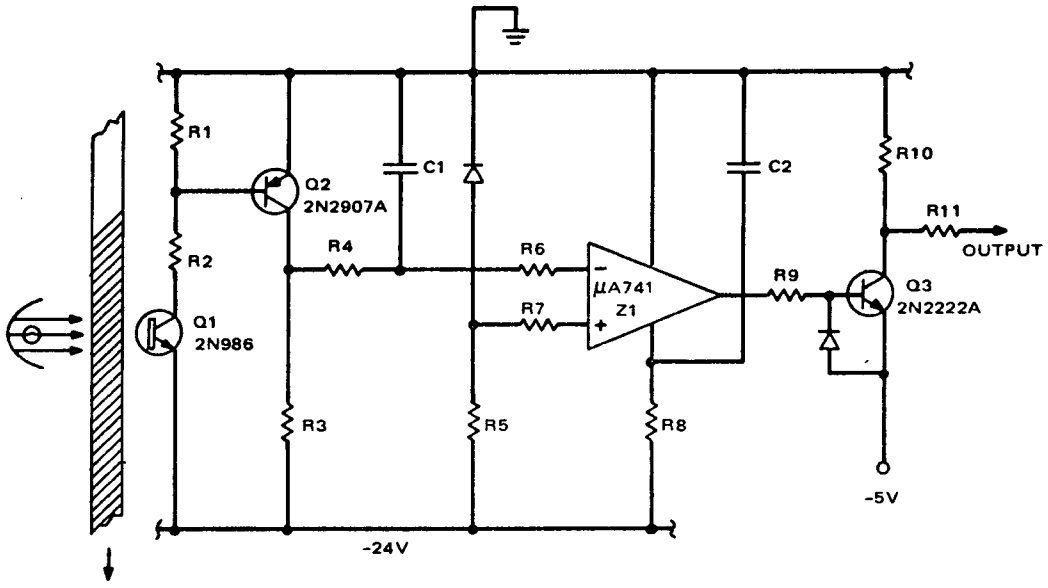


Figure 2-36. Optical End-of-Tape Configuration

The same circuit can be used for both ends of tape by using a timed inhibit circuit (one-shot). This allows the motor to run when the opposite direction command is received for a period long enough to allow the clear portion of tape to pass, before reactivating the sensing circuit.

2.2.2.3 Telemetry

The MCTR will provide the following telemetry data to the Data Processor:

(1) Command Status Telemetry Signal Type: 6 Level Analog
- V1 - OFF
- V2 - RECORD
- V3 - LOW SPEED PLAYBACK
- V4 - HIGH SPEED PLAYBACK
- V5 - CCW DIRECTION
- V6 - CW DIRECTION

(2) Motor Current Telemetry Signal Type: Analog

(3) EOT Status Telemetry Signal Type: 3 Level Analog
- V1 - NOT AT EOT
- V2 - EOT RECORD
- V3 - EOT PLAYBACK

(4) Pressure Telemetry Signal Type: Analog

(5) Temperature Telemetry Signal Type: Analog

2.2.2.4 Predicted Flutter

The frequencies at which the various elements of the MCTR begin resonating, creating changes in speed of the tape at the head, were determined with the aid of the analysis ECAP program (Electronic Circuit Analysis Program). First, an approximate torsional dynamic model was made from the MCTR mechanical schematics; diagrams of the models are shown in Figure 2-37 for the capstan-driven and Figure 2-38 for the reel-driven model. The inertia of the gears, reels, idlers, etc. and the stiffness constants for sections of magnetic tape, belts, elastic connection

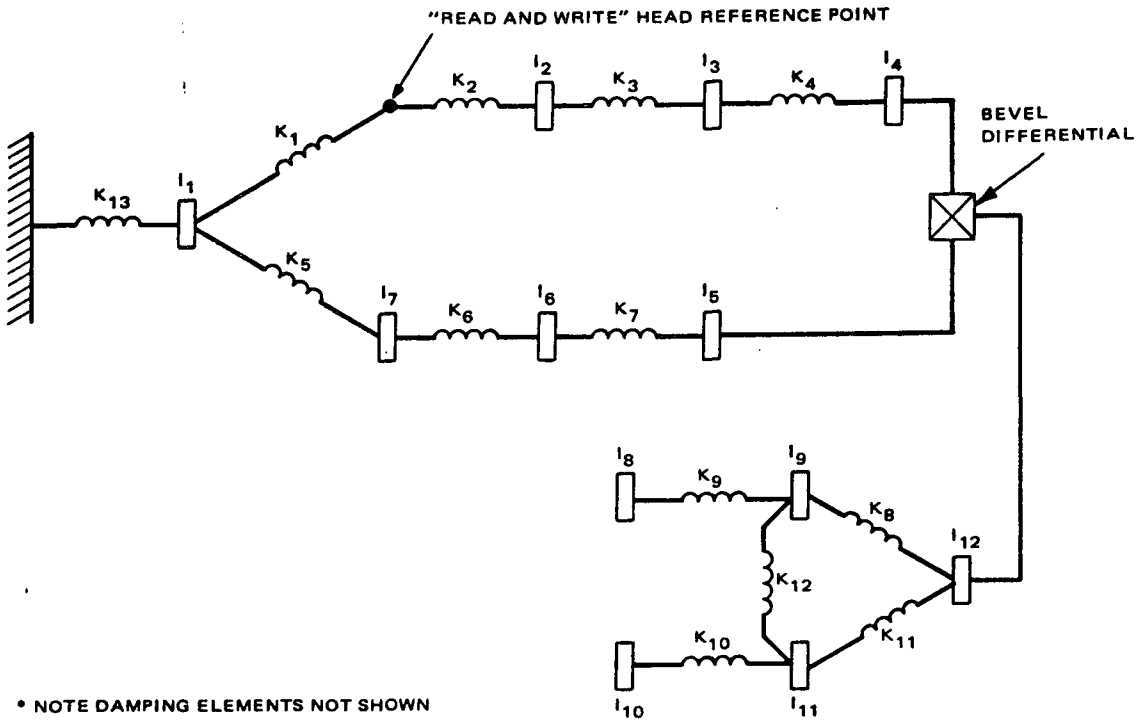


Figure 2-37. Capstan-Driven MCTR Torsional Dynamic Model

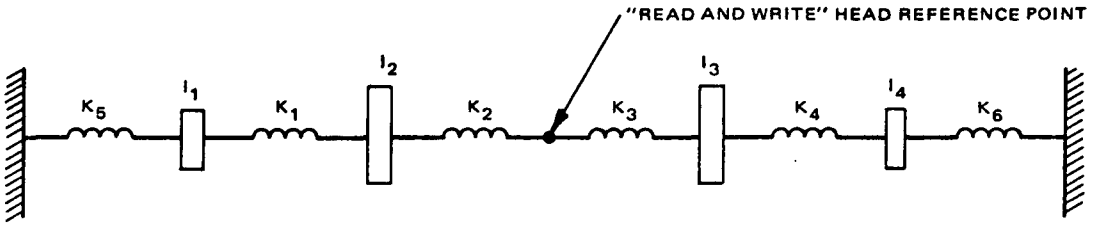


Figure 2-38. Reel Driven MCTR Torsional Dynamic Model

between magnetic field and motor, and springs were calculated. These values were then multiplied by appropriate reduction ratios which referred them back to the capstan or idler. Values for the capstan- and reel-driven models are listed in Tables 2-3 and 2-4. Electrical conversion factors (Figure 2-5) derived from dimensional analyses of the magnetic models* were then multiplied with the calculated mechanical values to obtain the electrical component values of the circuit. Resistor values representing the reciprocal of damping coefficients were computed by multiplying the quality factor, Q by the product of the inductance, the mid-band frequency of 1 Hz to 1 kHz (or 500 Hz), and 2 radians. The analog parameters are shown in Tables 2-5 and 2-6. The circuit was then determined from past knowledge of simple mechanical systems and their differential equations, which indicated how the electrical analog circuit was to be connected. An input of one volt, representing a speed of one radian per second, was applied to the circuit at the drive motor rotor at various frequencies. Logarithmic graphs of the voltage at the "Read and Write" head versus frequency were made. The peaks in the graphs (Figures 2-42 and 2-43) indicate the resonant frequencies at which flutter is at its worst. If the model is a good one, broad bandwidth noise in the system will give rise to peaks at these frequencies in the measured flutter spectra. If the spectral density of the noise has its own peaks, there will be peaks at those frequencies also. Typically, these will be at the capstan once-around frequency and at the motor-slot-induced torque ripple rate (see next section, 2.2.2.5). The prediction of the relative amplitude of the flutter peaks is much less precise than the prediction of the frequencies.

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*See Appendix D. (For the reader's convenience, Appendix D is included at the rear of this volume).

TABLE 2-3. PRIMARY TAPE TRANSPORT, CAPSTAN DRIVEN MCTR; TORSIONAL PARAMETERS, REFLECTED AT THE CAPSTAN

Element	Description	Inertia	
		lb in $sec^2 x10^{-6}$	Kg $m^2 x10^{-6}$
I_1	Capstan and Rotor	400	45.2
I_7, I_2	Idler	8.7	0.99
I_6, I_3	Reel, Reel shaft, and Reel Gear*	334	37.6
I_4	Differential gear system one	18.8	2.12
I_5	Differential gear system two	12.8	1.45
I_{10}, I_8	Storage spool*	183	20.7
I_{11}, I_9	Power drum*	333	37.24
I_{10}	Output differential gear*	7.98	0.9
Element	**Description**	**Stiffness**	
		lb in/rad	Nm/rad
K_1	Magnetic Tape Capstan to head	71.9	8.12
K_2	Magnetic tape head to idler	44.95	5.08
K_6, K_3	Magnetic tape idler to reel*	12.0	1.36
K_7, K_4	Neoprene belt reel gear to differential input gear one	3737.5	422
K_5	Magnetic tape capstan to idler	27.6	3.12
K_{11}, K_8	Neoprene belt output differential gear to drum*	500	56.5
K_{10}, K_9	Spring drum to spool*	12500	1413
K_{12}	Neoprene belt drum to drum*	1500	170
K_{13}	Motor magnetic field	17.7	2.0

* Values calculated at mid-tape; damping elements not shown.

TABLE 2-4. ALTERNATE TAPE TRANSPORT, REEL-DRIVEN MCTR; TORSIONAL PARAMETERS REFLECTED AT THE IDLERS

Element	Description	Inertia	
		$lb\ in\ sec^2 \times 10^{-6}$	$Kg\ m^2 \times 10^{-6}$
I_1	Motor and Reel[1]	171	19.3
	Motor and Reel[2]	310	35.1
	Motor and Reel[3]	669	75.6
I_2, I_3	Idler	3	0.34
I_4	Motor and Reel[1]	669	75.6
	Motor and Reel[2]	310	35.1
	Motor and Reel[3]	171	19.3
Element	**Description**	**Stiffness**	
		lb in/rad	Nm/rad
K_1	Magnetic tape reel to idler[1]	18	2.03
	Magnetic tape reel to idler[2]	22.5	2.54
	Magnetic Tape reel to idler[3]	36	4.06
K_2	Magnetic Tape Idler to head	30	3.39
K_3	Magnetic tape head to idler	45	5.08
K_4	Magnetic tape idler to reel[1]	36	4.06
	Magnetic tape idler to reel[2]	22.5	2.54
	Magnetic tape idler to reel[3]	18	2.03
K_5	Motor magnetic field[1]	0.168	0.019
	Motor magnetic field[2]	0.073	0.0082
	Motor magnetic field[3]	0.048	0.0054

1 Case One - one reel empty, the other full

2 Case Two - midtape

3 Case Three - one reel full, the other empty

* Damping elements not shown

TABLE 2-5. CAPSTAN DRIVEN MCTR ANALOG PARAMETERS

Component	Value	Analog
L_{1/R_1}	123mH/3860	Magnetic tape, capstan to head
L_{2/R_2}	196.8mH/6180	Magnetic tape, head to idler
$L_{6/R_6}, L_{3/R_3}$	735mH/23000	Magnetic tape, idler to reel
$L_{7/R_7}, L_{4/R_4}$	2.37mH/75	Neoprene belt, reel gear to differential input gear one
L_{5/R_5}	321mH/10050	Magnetic tape, capstan to idler
$L_{11/R_{11}}, L_{8/R_8}$	17.7mH/556	Neoprene belt, output differential gear to drum
$L_{10/R_{10}}, L_{9/R_9}$	0.71mH/22	Spring, drum to spool
$L_{12/R_{12}}$		Neoprene belt, drum to drum
$L_{13/R_{13}}$	0.5H/31.4K	Motor magnetic field
C_1	45.2 μF	Capstan and rotor inertia
C_7, C_2	1 μF	Idler inertia
C_6, C_3	37.6 μF	Reel, reel shaft, reel gear inertia
C_4	2.12 μF	Differential gear system one inertia
C_5	1.45 μF	Differential gear system two inertia
C_{10}, C_8	20.7 μF	Storage spool inertia
C_{11}, C_9	37.24 μF	Power drum inertia
C_{12}	0.9 μF	Output differential gear inertia

Note: R values calculated @ f = 500 hz and Q = 10, Q = 20 for belts and tapes, magnetic fields, respectively.

TABLE 2-6. REEL DRIVEN MCTR ANALOG PARAMETERS

Component	Value			Description
	Case One	Case Two	Case Three	
L_{1/R_1}	492mH/15.4K	394mH/12.4K	246mH/7.7K	magnetic tape, reel to idler stiffness/ damping
L_{2/R_2}	295mH/9.3K	295mH/9.3K	295mH/9.3K	magnetic tape, idler to head stiffness/ damping
L_{3/R_3}	197mH/6.2K	197mH/6.2K	197mH/6.2K	magnetic tape, head to idler stiffness/ damping
L_{4/R_4}	246mH/7.7K	394mH/12.4K	492mH/15.4K	magnetic tape, idler to reel stiffness/ damping
L_5	54H	121.5H	184.5H	Motor magnetic field stiffness*
C_1	19.3μF	35.1μF	75.6μF	Reel and motor inertia
C_2, C_3	0.34μF	0.34μF	0.34μF	Idler inertia
C_4	75.6μF	35.1μF	19.3μF	Reel and motor inertia

Note: R values calculated @ f = 500 Hz and Q = 10 for tapes, Q = 20 for fields.

*Damping resistance for the motor field has been neglected.

One-to-One Model Ratio

Voltage = velocity

$$\text{Volts} = \frac{\text{RAD}}{\text{SEC.}}$$

Current = Torque

Amps = Nm = 0.113 lbf. in

$$\text{Resistance} = \frac{1}{\text{rotational damping}} = \frac{1}{\text{torque/velocity}}$$

$$\text{Ohms} = \frac{\text{RAD/SEC}}{\text{Nm}} = 8.85\ \frac{\text{RAD/SEC}}{\text{lbf. in}}$$

$$\text{Inductance} = \frac{1}{\text{Rotational stiffness}} = \frac{1}{\text{torque/rad}}$$

$$\text{Henrys} = \frac{\text{RAD}}{\text{Nm}} = 8.85\ \frac{\text{RAD}}{\text{lbf. in}}$$

Capacitance = Inertia

$$\text{Farads} = \text{kg} \cdot \text{m}^2 = 0.113\ \text{lbf. in} \cdot \text{sec}^2$$

Figure 2-39. Electromechanical Conversion Factors

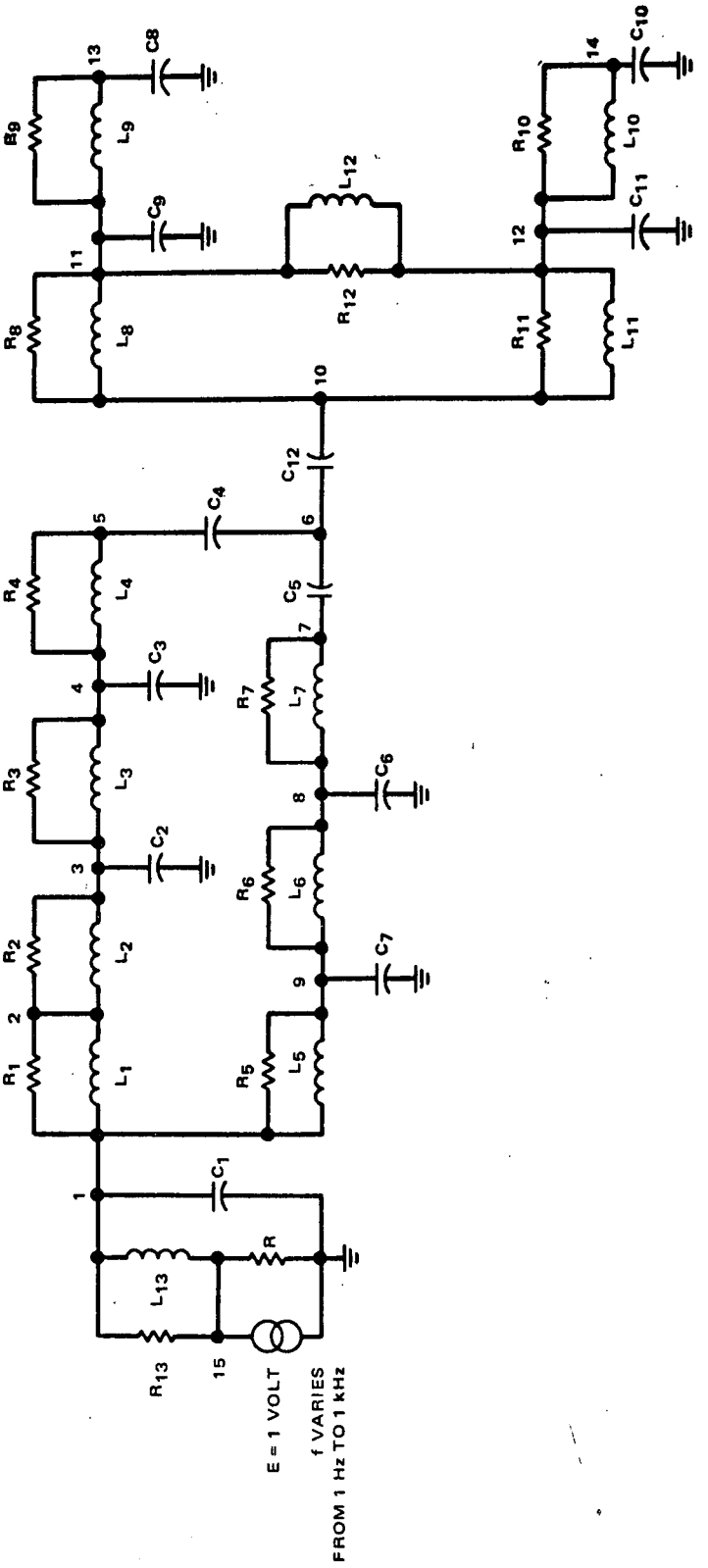

Figure 2-40. Capstan Driven MCTR Magnetic Model

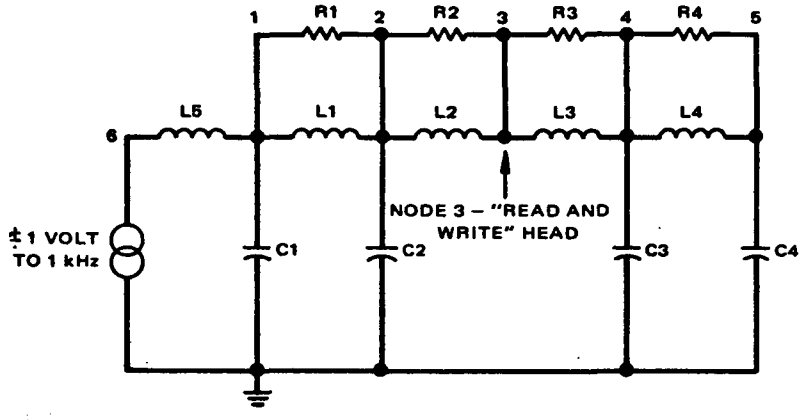

Figure 2-41. Reel-Driven MCTR Magnetic Model

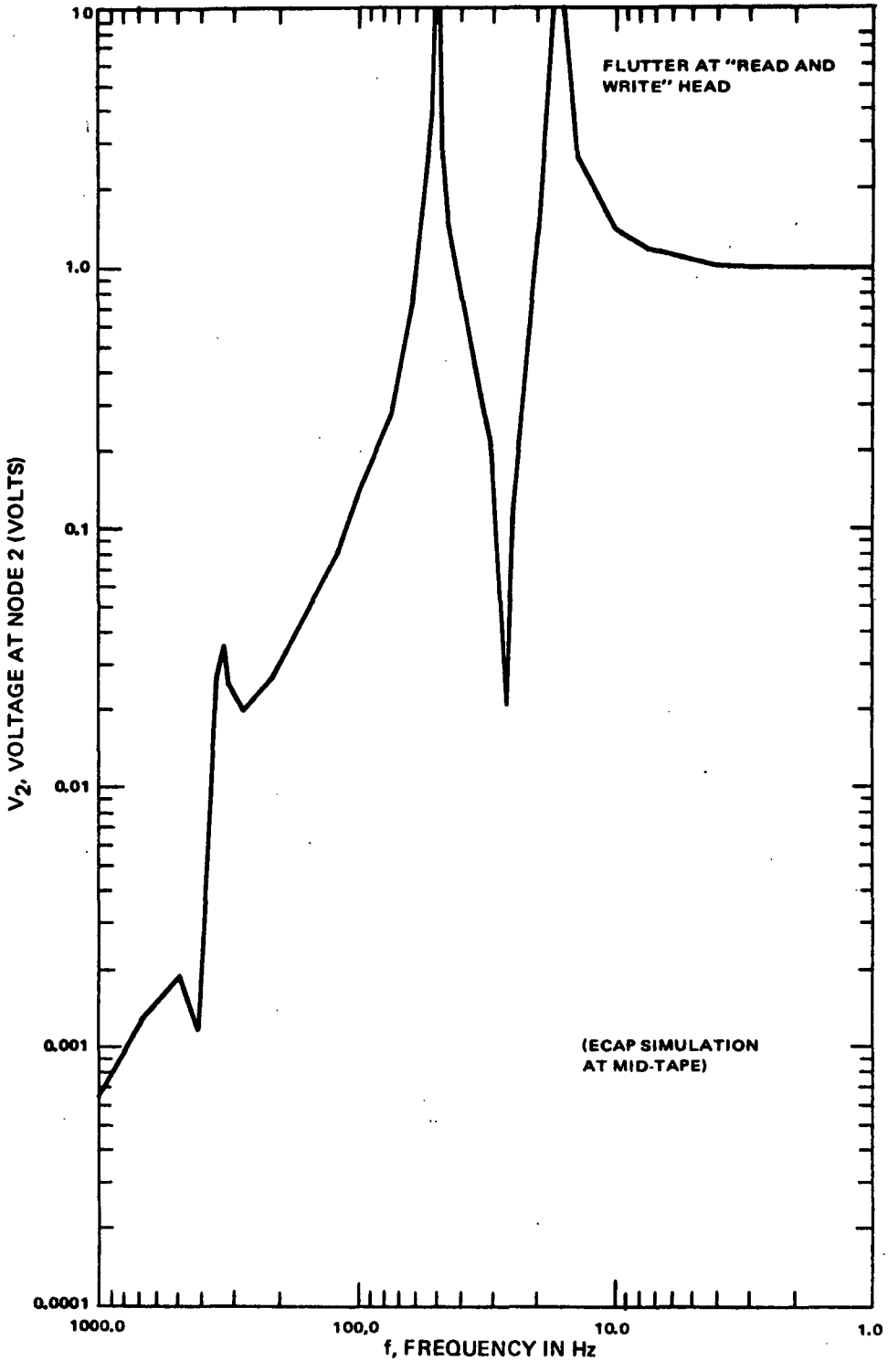

Figure 2-42. Capstan-Driven MCTR Electrical Analog Flutter at "Read and Write" Head (ECAP Simulation)

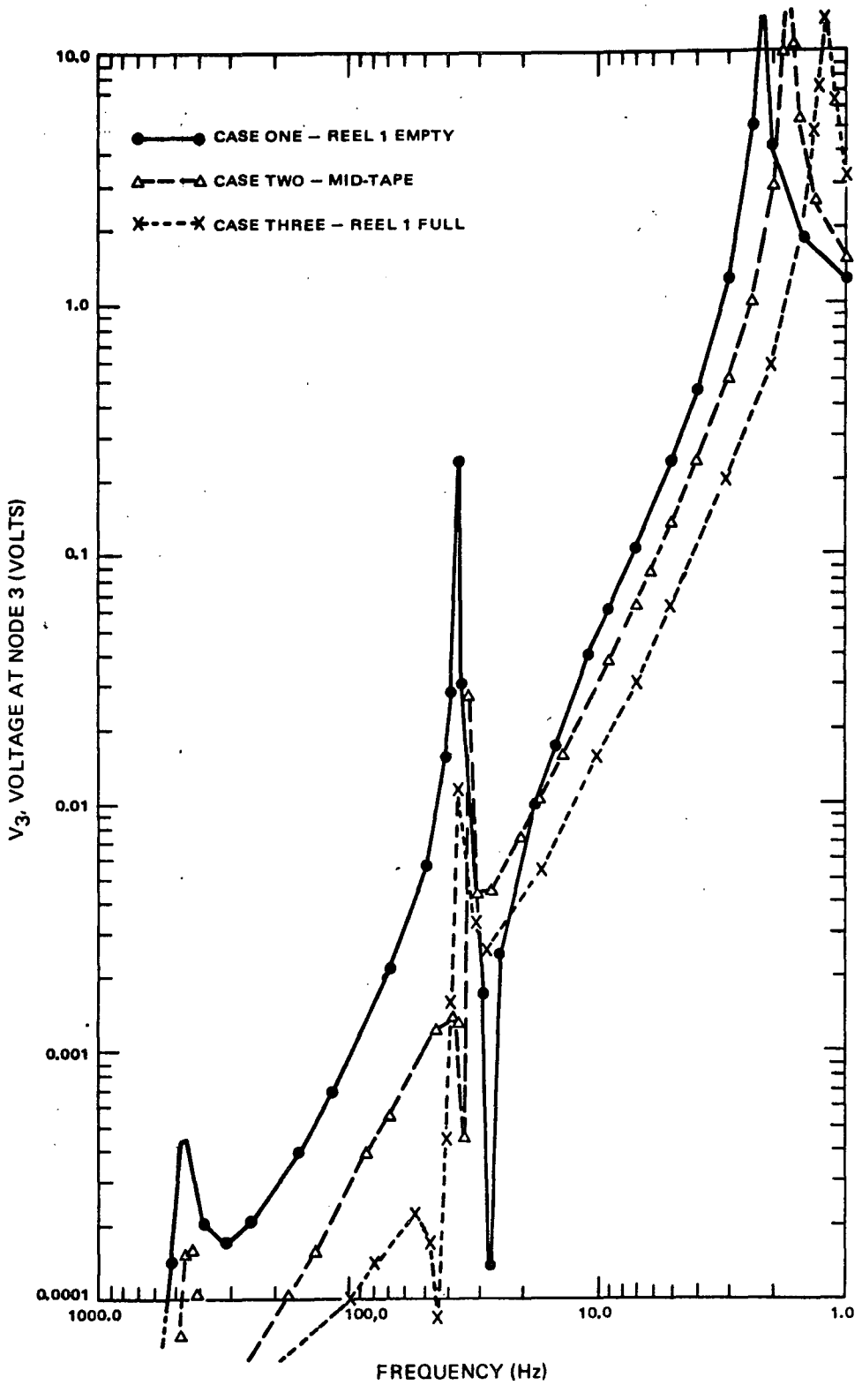

Figure 2-43. Reel-Driven MCTR Electrical Analog Flutter at "Read and Write" Head (ECAP Simulation)

2.2.2.5 Servo Loop Analysis

2.2.2.5.a Capstan-Driven Recorder Loop Analysis

A block diagram for the MCTR capstan-driver is shown in Figure 1 of Appendix E. The diagram does not include the feedback loop, which controls the motor terminal voltage E to maintain constant playback or record speed. The motor constants are defined on page 2 of Appendix E. Equations 1 through 7 on pages 2 and 3 of the Appendix allow the motor diagram to be reduced to that shown in Figure 2. This reduction is simplified by the valid assumption that the motor electrical time constant is much lower than the time constant due to motor-load inertia, as exemplified by the constants shown for the MacBar brushless motor typical of the type to be used. This simplified representation of the motor-load combination is used in conjunction with a phase detector, lead-lag compensation circuit, pulse-width modulator, and motor drive power amplifier to complete the servo loop, shown in Figure 3 of Appendix E. The phase detector compares the capstan position with a clock reference and creates an error signal to drive the servo. The lead-lag compensation shapes the gain-phase response to provide closed-loop stability with adequate bandwidth. The pulse-width modulator (PWM) uses a constant-frequency sawtooth and a comparator to generate a rectangular wave, the duty cycle of which is modified as a function of the error signal. The rectangular wave, in turn, drives the motor by means of a separate power amplifier for each winding.

Sheet 6 of Appendix E shows the transfer functions for open-loop gain, flutter response due to torque disturbances, and the time integral of flutter, known as jitter or displacement error. The jitter response is meaningful since it can be directly related to the bit error based upon an assumed percentage torque disturbance and practical bit packing density.

2.2.2.5.aa Computer Results

(All computer results are in Appendix F.)

A plot of flutter in radians per second per Newton-meter torque disturbance versus frequency is shown in Figure 1 of Appendix F for the mid-tape case. The once-per-revolution frequencies for the reel and capstan have been indicated, with the lower frequency representing record mode and the higher frequency playback mode, in each case. The slot ripple frequencies for the motor (48 times the once-per-revolution rate) have also been indicated. Flutter is more likely to occur at the frequencies shown, but may also occur at rates equal to harmonics of the basic frequency, although probably much reduced.

Flutter amplitude expressed in radians per second has meaning for analog signals when demodulated, but for digital signals, the length of tape displaced by a torque disturbance can be related directly to a specific number of bits. This bit error is determined by integrating with time the flutter response as shown in Figure 2 of Appendix F. The displacement scale of radians per Newton-meter can be converted to bits by assuming a disturbance error equal to 10 percent of the load torque at 2.4 Newtons differential tension with a 15-mm-diameter capstan as follows:

$$\text{Torque Error} = 0.1.2.4 \cdot \frac{15}{2} \cdot 10^{-3} = 1.8 \cdot 10^{-3} \text{N m}$$

With a packing density of 800,000 bits per meter (20,000 bits per inch), one radian of angular distance of a 15-mm capstan presents 6000 bits. The radians per Newton-meter scale is converted by a factor K as follows:

$$K = 0.0018 \text{ N}\cdot\text{m} \cdot 6000 \frac{\text{Bits}}{\text{Rad}} = 10.8 \frac{\text{Bits}}{\text{Rad/N}\cdot\text{m}}$$

The jitter response as shown in Figure 2 of Appendix F has a maximum bit error of 0.07 at low frequencies and drops to even lower errors at 10 Hz and above.

2.2.2.5.b Alternate Recorder Loop Analysis (Reel-Driven)

A block diagram for the MCTR reel drive system is shown in

Figure 1 of Appendix G* This does not include the feedback loop, which controls speed by reading a previously recorded clock signal at the playback head, comparing it to a reference, and controlling motor-terminal voltage. The block diagram is manipulated, as shown on pp 2 and 3 of Appendix G to produce the simplified reel motor-to-tape head transfer function (Figure 2).

The blocks f1(S) and f2(S) represent the torque-to-velocity transfer functions at the reel and head respectively. The transfer functions are derived from an electrical and analog of the mechanical model as shown in Figure 3 of Appendix G, with the driving reel radial velocity indicated by the voltage across C1 and the velocity at the head (expressed in radians per second, referenced to a one-inch-diameter idler) by the voltage across R, where R is the tape drag across the head. The capacitances represent reel and idler inertias, and the inductances, tape stiffness between the points indicated in Figure 3.

Pages 5 and 6 of Appendix G show that f1(S) and f2(S) transfer functions with the assumptions and simplifications of page 6 included. Values for R, L, and C for the following three cases are also included: start-of-tape, mid-tape, and end-of-tape.

The complete servo block diagram is shown in Figure 4 of Appendix G and includes the pulse-width-modulator and power switches for driving the motor, lead-lag compensation for extending the bandwidth and providing adequate closed-loop phase margin, a phase detector for comparing angular position of the recorded signal with an encoder reference signal and producing a dc error voltage to operate the PWM, and an integrator to translate angular velocity at the tape head to angular position, in addition to the reel-drive system described previously.

On sheet 6 of Appendix G are the transfer functions for open-loop gain, flutter at the tape head due to torque disturbance at the reel, and jitter, which is the time integral of flutter. The jitter response can be directly related to the bit error based

*For the reader's convenience, Appendix G is included at the rear of this volume.

on an assumed percentage torque disturbance and practical bit packing density, as explained previously in Appendix E.

2.2.2.5ba Servo Loop Development and Computer Results
(All computer results are in Appendix F)

The system was first configured with one-inch idlers and minimal reel-to-idler and idler-to-head tape distances. Figure 3 of Appendix F shows the mid-tape, uncompensated, open-loop gain and phase response (Bode plot) with 10.2 dB of gain at the 180-degree, phase-shift point, resulting in an unstable system. Figure 4 is the same plot with 10-Hz to 100-Hz lead-lag compensation included and shows a conditionally stable condition. The resultant flutter in radians per second per Newton-meter is shown in Figure 5 with the lead-lag compensation of Figure 4. A flutter peak of 178 radians per second per Newton-meter is reached at 199.5 Hz, which is close to the playback-motor slot-ripple frequency.

Since the open-loop response was conditionally stable with only 7 degrees of phase margin, it was decided to reduce the gain by 20:1; thereby allowing 50 degrees of phase margin and 26.7 dB of gain margin, as shown in Figure 6. The high-frequency flutter peak narrowed considerably (Figure 7) but a broad lower-frequency peak developed due to the reduced bandwidth.

At this point, the idlers were reduced to one-half-inch diameter to increase their resonance frequency (decreased inertia) evidenced by the response peak shown in the previous Bode plots. The 10-Hz to 100-Hz lead-lag compensation was maintained, but with a gain reduction of 2:1 included. With these conditions, the bandwidth was extended to 84.1 Hz (as opposed to 12.6 Hz with one-inch idlers) with 34 degrees phase margin and 12.4 dB of gain margin, as shown in Figure 8. Figure 9 shows the corresponding flutter response.

At this point in the development of the system, an error was discovered in one of the coefficients for the transfer functions f1(S) and f2(S) and so it was decided to rerun the one-half-inch idler, uncompensated, open-loop response for three conditions of

reel inertia, i.e., start-of-tape, mid-tape, and end-of-tape. This is shown in Figures 10, 11, and 12 respectively. All three cases were unstable, as before, with the end-of-tape case presenting the greatest amount of negative-gain margin: -12.1 dB. The idler inertia peaking was again evident, but at a much higher frequency, as expected for the 4:1 decrease in inertia. It appeared that the 10-Hz to 100-Hz lead-lag compensation was proper and the cases were rerun with the compensation included as Figures 13, 14, and 15 of Appendix F. From these Bode plots it was possible to determine the amount of gain reduction necessary to achieve 35-degree phase margin, which is considered adequate for loop stability and at the same time allows the system to be responsive to transients. This ranges from 0.19 (-14.4 dB) at the start of tape to 0.82 (-1.7 dB) at the end of tape. Plots of flutter attenuation for each of the three cases and with the aforementioned gain reduction included are shown in Figures 16, 17, and 18 of Appendix F. Indicated on the plots are the frequencies at which the once-per-revolution reel and idler and the 48-times-per-revolution motor-slot-torque ripples occur. The slot ripple is specified as 0.12 ounce-inch, 0-to-peak ($8.5 \cdot 10^{-4}$ N·m) which results in a 0.025-radian-per-second 0-to-peak flutter amplitude at the 67-Hz rate during record mode and 0.015-radian-per-second 0-to-peak flutter at the 200-Hz playback rate start-of-tape. No torque numbers have been determined for reel and idler perturbations, but these effects should be minimal.

A more meaningful effect of a torque disturbance is the bit error or jitter determined by the time integral of the flutter response. This is shown in Figures 19, 20, and 21 of Appendix F for the three cases where the left-side scale is expressed in radians per Newton-meter. If a nominal tape tension of 2.54 Newtons (9 ounces) is selected, this converts to a load torque of 0.032 Newton-meter when referred to a one-inch-diameter idler. With a packing density of 800,000 bits per meter (20,000 bits per inch), one radian of angular distance of a one-inch idler represents 10,200 bits. If a

disturbance torque equal to 10 percent of the load torque is assumed (0.0032 N·m), then the radians per Newton-meter scale can be converted to bits by a conversion factor K as follows:

$$K = 0.0032 \text{ N·m·10,200} \frac{\text{Bits}}{\text{Rad}} = 32.6 \frac{\text{Bits}}{\text{Rad/N} \cdot \text{m}}$$

The jitter response from Figures 19, 20, and 21 of Appendix F ranges from 4.3 bits at end of tape to 10 bits at the start of tape, well within the capabilities of the storage register when combined with the expected skewing error.

2.2.2.6 EMI

The MCTR will be designed to operate without interference in the EMI environment of a satellite containing both EMI-sensitive units and EMI generation units. The following tests, per MIL-STD-462, are typical requirements for satellite subsystems:

Conducted Interference (Power Lines)	DC to 20 MHz
Conducted Susceptibility (Power Lines)	30 Hz to 400 MHz
Radiated Interference	14 kHz to 2 GHz
Radiated Susceptibility	14 kHz to 2 GHz

Portions of the preceding may not be applicable to the MCTR, such as the radiated susceptibility requirement for the proposed brushless motor.

2.2.2.7 Power Transients

The MCTR will be designed to withstand, without damage or impairment of component life, low-repetition-rate transients on the power-supply lines such as the following:

- Loss of power, due possibly to contact bounce in a power-line relay, during which time the line will vary from the supply voltage to an open condition.
- Loss of power, due to switchover to a redundant power supply, during which time the line may vary from the supply voltage to a low voltage at low impedance and back to the supply voltage.
- Excessive high voltage, due possibly to momentary loss of regulation.

The tape recorder will operate within specification and exhibit not degradation of life after return to normal operating voltage.

The MCTR will also be protected against and perform within specifications with a voltage sine or square wave superimposed on any power input. A typical waveform might be 0.5 V peak-to-peak square wave with a 10 second rise-fall time at a 1-kHz rate.

2.2.3 Analog Signal Processing

2.2.3.1 Recording Method

The recording method selected is that of constant-current, saturation recording without high-frequency (ac) bias. The alternative method considered was recording with ac bias. The tradeoff involved with ac bias is extended-playback, high-frequency response as against the additional size, weight, and power consumption. As a minimum, a record-with-bias system would require a master bias square wave oscillator and 112 amplifier-shapers. Amplifier-shapers are necessary to generate 112 independent sine-wave bias signals. This will avoid inter-channel crosstalk that could occur through use of a common bias-supply system. Because of the need for a considerable number of electronic parts and an additional penalty of three to five watts of record power, record-with-bias is not considered feasible for this recorder system.

2.2.3.2 Erasing Technique

A separate, full-track, dc, magnetic erase head will be used. It will be programmed to erase during a normal playback-mode pass. It is desired to make the erase programmable to provide for repetitive playback passes and rewinds.

2.2.3.3 Record Head

A single head (Figure 2-44) will be used for both the record and playback function. The use of a single head reduces timing errors caused by skew since static skew components due to gap scatter and azimuth alignment will be eliminated.

2.2.3.4 Playback Signal

2.2.3.4a Delay Code Spectral Density Characteristics

Figure 2-45 shows a worst-case word in delay code format that must be processed by the recorder. A biphase level format is shown for comparison purposes. Over a two bit cell period (11), biphase data requires four flux reversals (transitions) on magnetic tape for proper storage. With delay code, only two flux reversals are required to store the same two bits of data. Expressed in the frequency domain, delay code has a two-bit-per-cycle capability as compared to a one-bit-per-cycle for biphase. For a given magnetic-

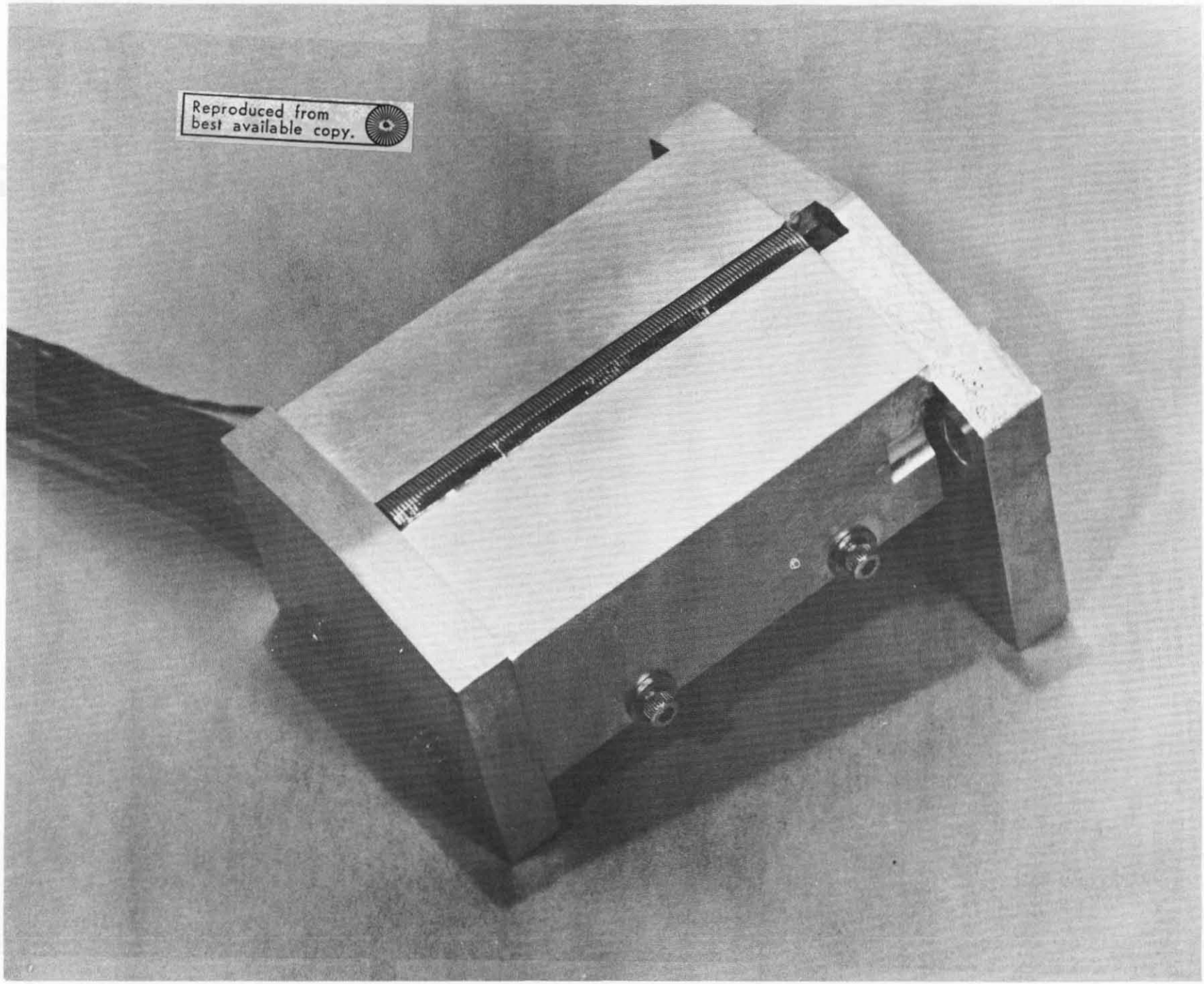

Figure 2-44. Record-Playback Head

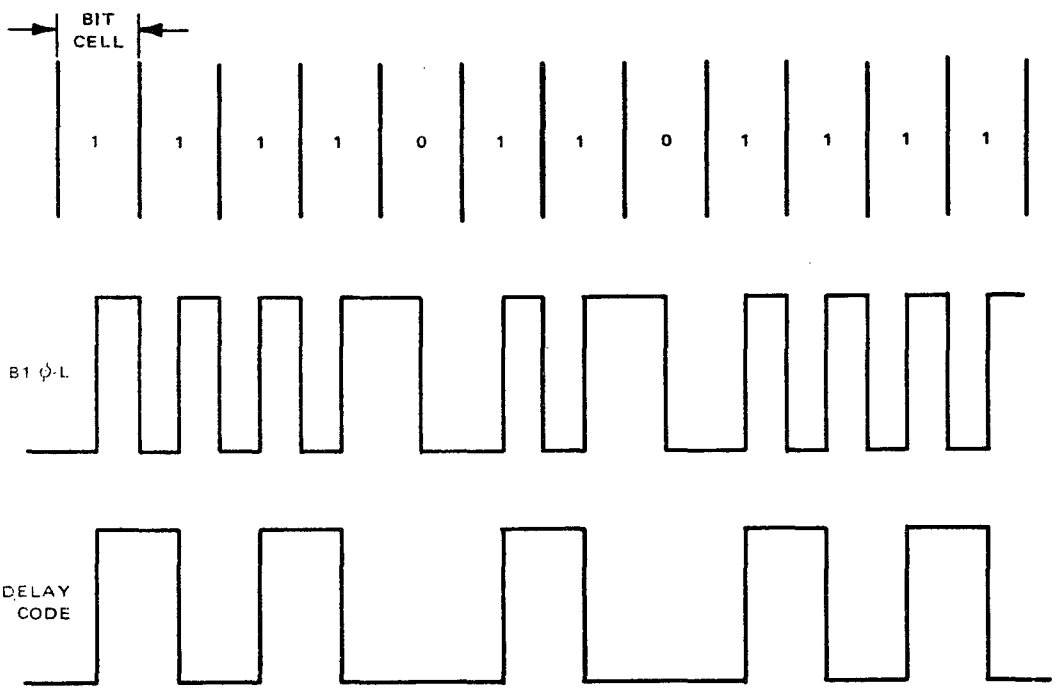

Figure 2-45. Delay Code Format

tape-recorder frequency-response characteristic, twice as many bits per linear inch of tape can be stored using delay code as against conventional biphase, without increasing the transition packing density on the tape.

A plot of spectral density in watts per hertz for a typical delay code word is shown in Figure 2-46. Superimposed on the plot is the calculated and RCA measured head-tape frequency response for the baseline high-density recorder (low-speed, low-speed). The peak power for delay code occurs at 0.38 of the bit rate (167 kHz). This corresponds to a wavelength of 3.4 μm (135 μinch). The ratio of this wavelength to the playback head mechanical gap is 0.27. Minimum required bandwidth for adequate data processing extends from 0.05 bit rate (22 kHz) to 0.7 bit rate (308 kHz).

Clearly shown in the spectral-density plot is the non-zero dc response, which is characteristic of delay code. This is illustrated by Figure 2-47. When the delay code word of 101101 is both preceded and followed by all ones, the result will be a waveshape with an average dc level. In playback, the reproduce head cannot respond to the dc component in the waveshape. The over-all result will be some amount of zero-crossing baseline shift in the playback waveshape. For a given recorder head-tape response, the severity of the baseline shift will be essentially a function of the operating bit-packing density.

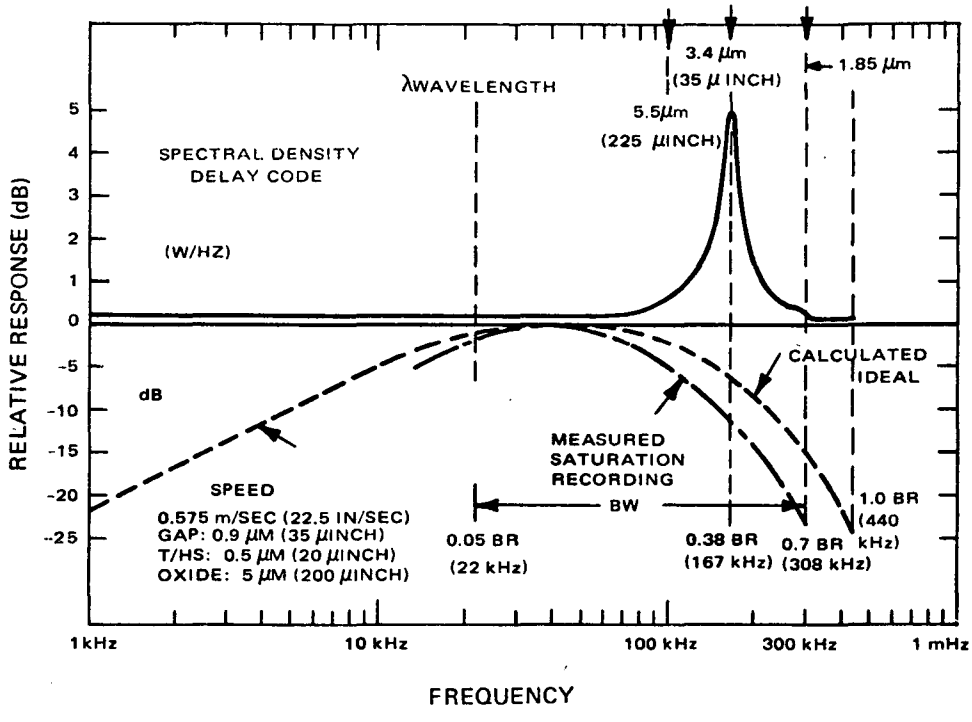

Figure 2-46. Spectral Density of Data vs Frequency

$$E_o = K\left[\left(\frac{\sin \pi X_g/X_L}{\pi X_g/X_L}\right)\left(\frac{5-4(X_L/X_g)^2}{4-4(X_L/X_g)^2}\right)\right]\left[e^{-2\pi X_D/X_L}\right]\left[1-e^{-2\pi X_o/X_L}\right]$$

K = Constant dependent on track width/head

K_g = Playback head mechanical gap width

X_L = Recorded wavelength $\left(\frac{\text{Tape Speed}}{\text{Frequency}}\right)$

X_D = Head-to-tape oxide separation (surface)

X_o = Tape oxide thickness

Figure 2-47. Ideal Head-Tape Response Playback Equation (Sinusoidal, Optimum Value)

2.2.3.4.b Equalizing to Minimize Zero-Crossing Errors

An existing RCA computer-simulation program was used to predict the zero-crossing errors expected when processing delay-code data through the recorder.

Zero-crossing errors in playback at high packing densities are the result of two conditions. The first is the time-base-line shift due to pulse crowding effects. That is, pulse interference in playback caused by a very close spacing between two adjacent flux reversals recorded on the tape using saturation recording. The second condition will be the time-base shift caused by the dc component in the delay-code waveshape.

The digital computer program essentially involves calculating the effect of passing digital NRZ-type data waveshapes through band-limited networks. In this case, both the magnetic record-reproduce process and the equalizer are each represented as bandpass filters with a known transfer function. The recorder playback simulation was divided into two parts: non-equalized and equalized.

Figure 2-48 (B,C) shows the transfer function for the expected head-tape amplitude and phase characteristic. Based on RCA experience, the upper frequency response characteristic (B) was degraded -6db over the ideal calculated curve (A). This is to account for pulse crowding effects caused by using NRZ saturation recording at short wavelengths - less than 12.7 μm (0.5 mil). A 44-bit delay code word with the characteristic 101101 inserted in the center portion (Figure 2-49) and a 0.5 bit rate centered at 225 kHz was selected. This simulates a bit packing density of 0.8 megabit per meter (20 kilobits per linear inch) of tape.

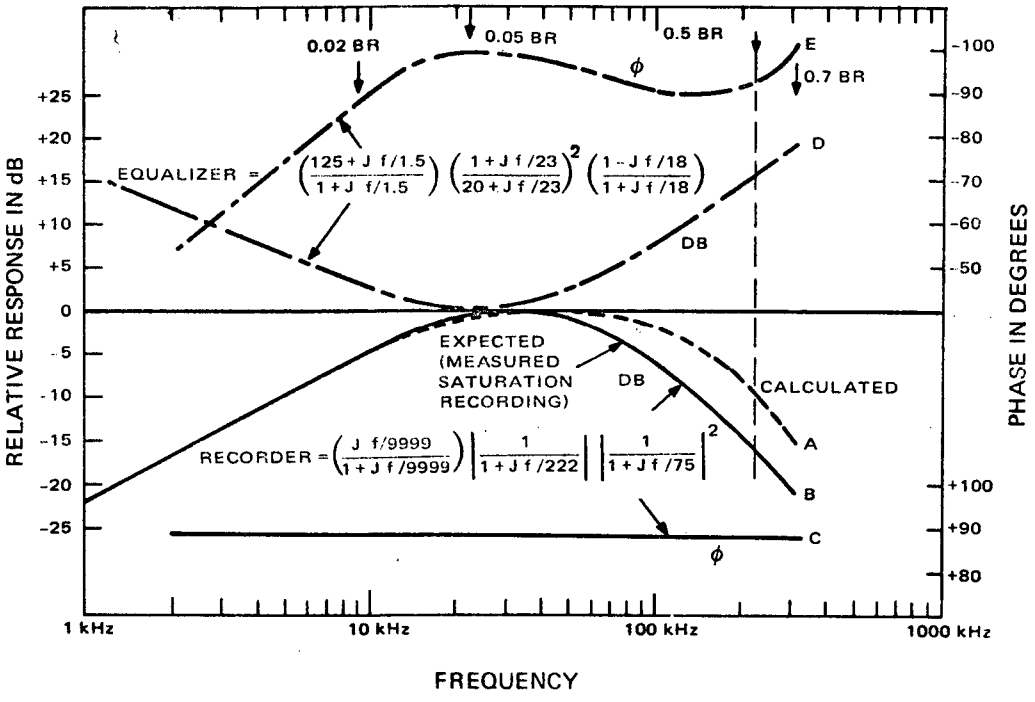

Figure 2-48. Transfer Functions for Primary MCTR; 0.575 m/s (22.5 in/s), Record and Playback

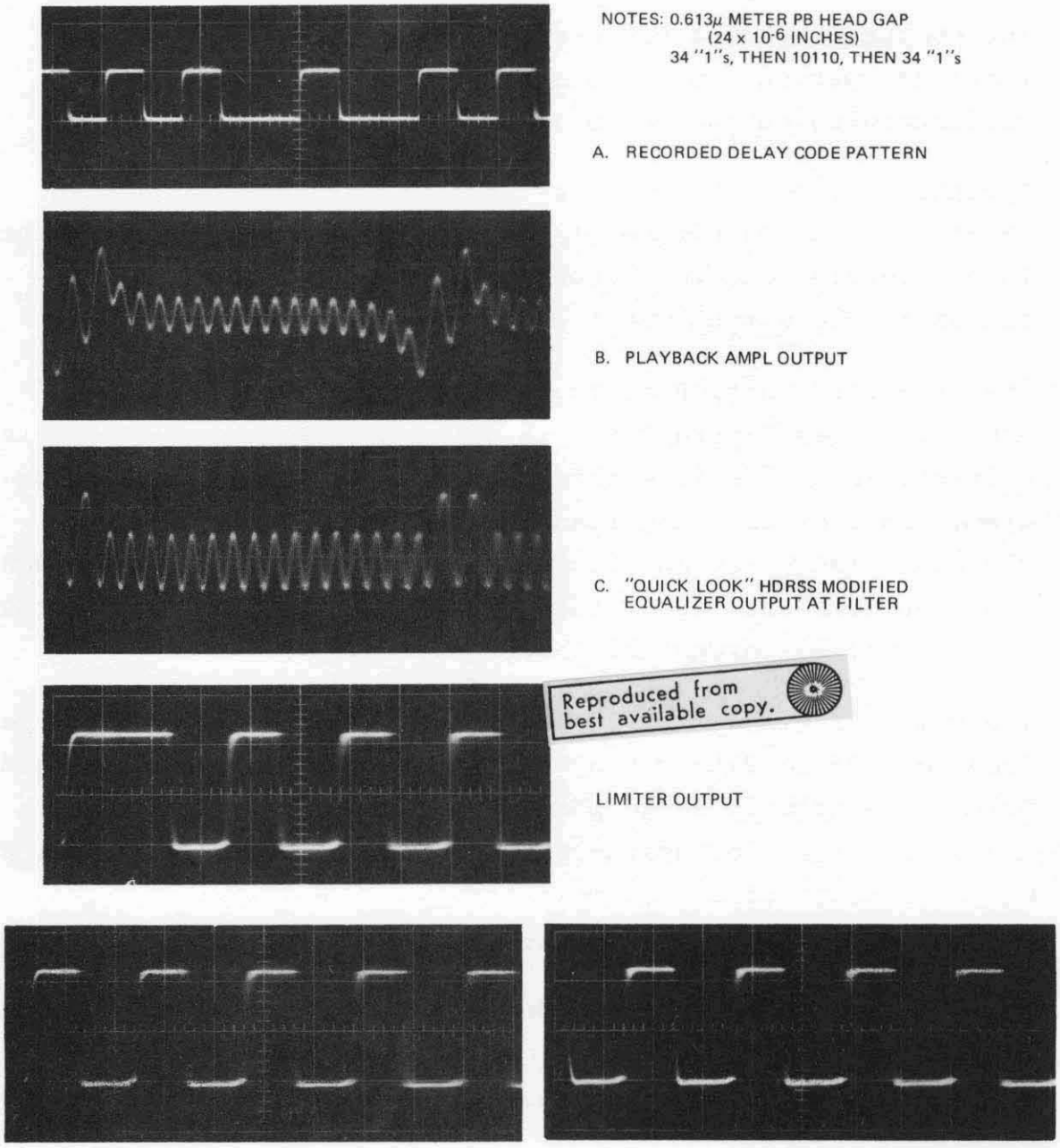

Figure 2-49. Delay Code Wave Shapes, 0.8 Mb/m (20 kb/in.)

The computer readout processing this data word consists of tabulated percent zero-crossing errors and a plot of the corresponding output waveshape.

Appendix H shows the computer readout for the unequalized recorder. The magnitude of the baseline shift is sufficient to completely lose zero-crossing identity in two separate places in the output waveform plot.

The transfer function of the inductorless zero crossing equalizer (see Figure 2-51) is plotted in Figure 2-47. This characteristic was inserted in the computer simulation program, and the resulting readout is shown in Appendix I. The plot clearly shows the restoration of the zero crossings. The tabulated data shows that the zero crossings were corrected to within 2.13 percent of their true value.

The computer simulation program indicates that 20-kilobit-per-inch delay-code data can be adequately processed by a recorder, using a relatively large playback gap of 0.9μm (3.5 μinch), and a resistance-capacitance type of amplitude-phase equalizer with a minimum circuit complexity.

Verification of the computer program technique is shown by the photographs of Figure 2-49. Picture B shows the baseline shift and the resulting loss of zero crossing identity in two places. Picture C shows the restoration of the zero crossings by the equalizer.

Figure 2-50 shows the transfer functions for the alternate recorder; low-speed record and high-speed playback. Computer runs based on these functions produced the identical results shown for the baseline recorder.

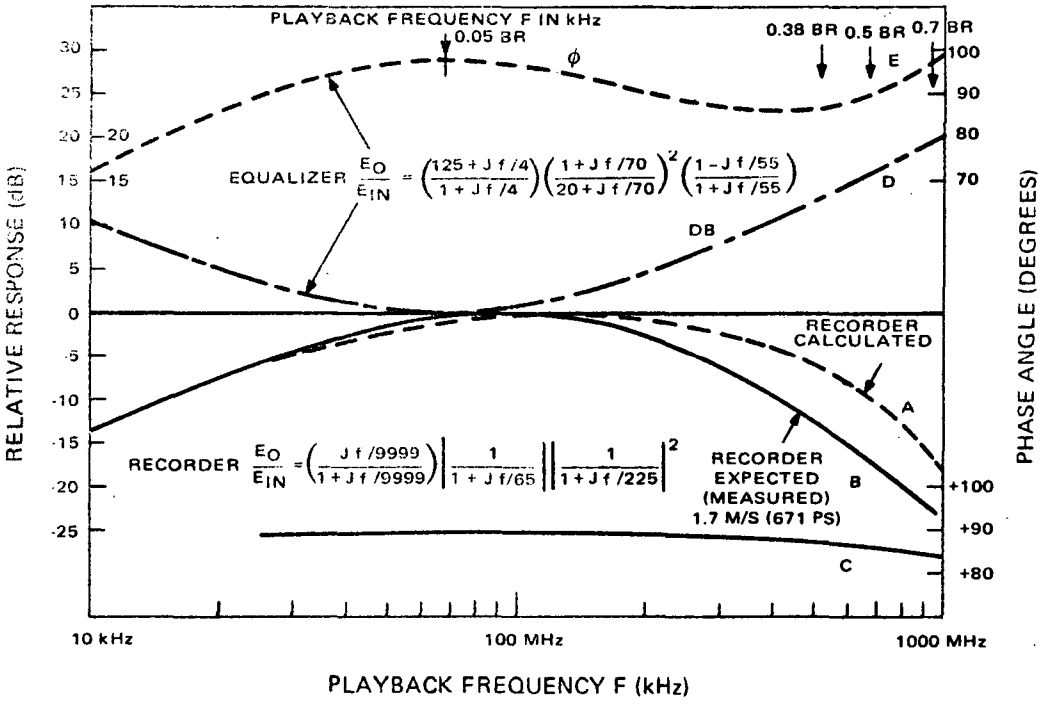

Figure 2-50. Transfer Functions for Alternate MCTR; 0.575 m/s (22.5 in/s) Record, 1.72 m/s (67 in/s) Playback

2.2.3.4.c Intertrack Crosstalk

Intertrack crosstalk is the result of two factors. The first is simple magnetic coupling between individual head tracks. The second is due to the lateral sensitivity of the head in playback. Intertrack magnetic coupling is a head design problem and is minimized by shielding techniques. Lateral sensitivity can be treated like a head-to-tape-track separation loss, and the same basic relationship applies;

$$54.6 \quad \frac{\text{(distance track edge to edge)}}{\text{(wavelength)}} \text{ dB.}$$

At 100 kHz, 0.575 m per second (22.5 in.per second) and 0.22 mm (0.00 in.) track-edge spacing, the lateral crosstalk calculates out to greater than 1000 dB, assuming perfect tape tracking. The calculation shows that crosstalk due to magnetic coupling only directly at the head needs to be considered.

RCA has conducted interchannel crosstalk measuring tests using a reproduce head with a 0.3mm (0.012 in.) track width and a 0.9 mm (0.036 in.) track spacing. At 100 kHz, 40 db peak-to-peak/ peak-to-peak minimum was measured. This corresponds to a value of 46 db peak-to-peak/rms. The manufacturer of the specific head used guarantees at least -35db of interchannel crosstalk. With a track spacing of 0.5mm (0.02 in.) (to achieve the capability of 112 tracks) the -35db figure is feasible.

2.2.3.4.d Playback Signal Processing Electronics

2.2.3.4.da General

Figure 2-51 (B) shows a block diagram of the proposed electronics to reproduce the recorded delay-code data. The basic method used is to amplitude and phase equalize the playback data to restore zero-crossing identity

lost in the magnetic reproduction process. Ideal magnetic reproduction involves generating a voltage waveshape that is the differential with respect to time of the recorded flux on the tape. In the frequency domain, this produces a +6dB per octave amplitude response with a constant +90-degree phase shift. As the recorded-signal wavelength decreases, the reproduce-head gap width, head-to-tape oxide separation, and oxide-thickness losses all react to roll off the amplitude response (see Figure 2-50). The first null, or zero amplitude, will occur essentially when the recorded wavelength equals 85 percent of the playback head mechanical gap width. This corresponds to a playback frequency of 5.46 kHz.

2.2.3.4.db Zero-Crossing Equalizer

Ideal equalization for the record-playback process involves the design of a network with an amplitude-vs-frequency characteristic of -6dB per octave at long wavelengths, 12 to 18 dB per octave at short wavelengths, and an overall constant phase shift of 90 degrees.

Figure 2-52 shows a three-stage, inductorless amplitude-phase equalizer. It is composed of one active RC integrator stage, two active RC differentiator stages, and one all-pass RC network stage. The resulting amplitude-phase response is shown in Figure 2-49. The use of RC network equalization over inductor-type networks is dictated by minimum weight and size considerations, since 112 such equalizers are required.

2.2.3.4.dc Linear Phase Filtering

The 12-dB per octave peaking at the higher frequencies introduced by the equalizer will degrade the playback signal-to-noise ratio. A low-pass filter with linear phase (constant envelope delay) will restore the major portion of the pre-equalized signal-to-noise ratio without degrading

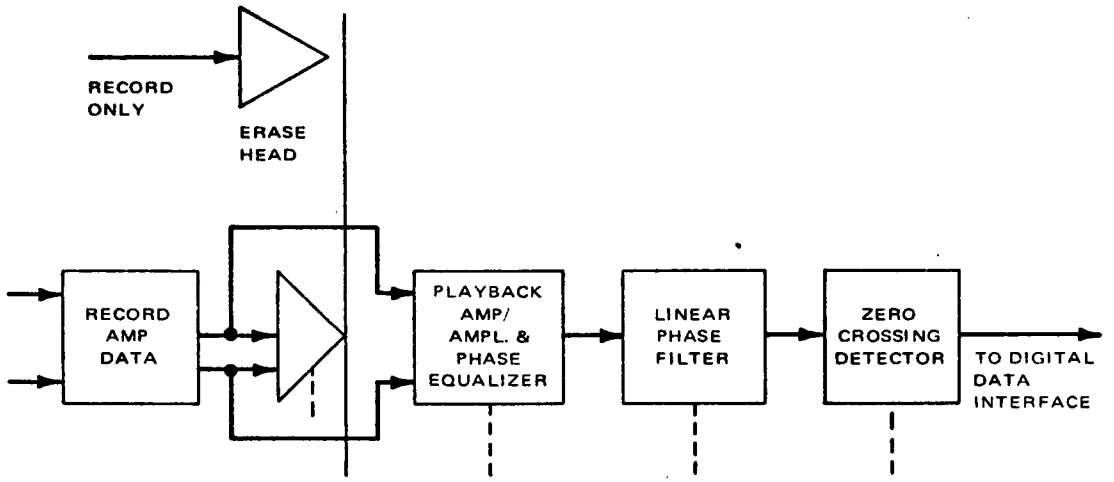

Figure 2-51. Proposed Playback Electronics Block Diagram

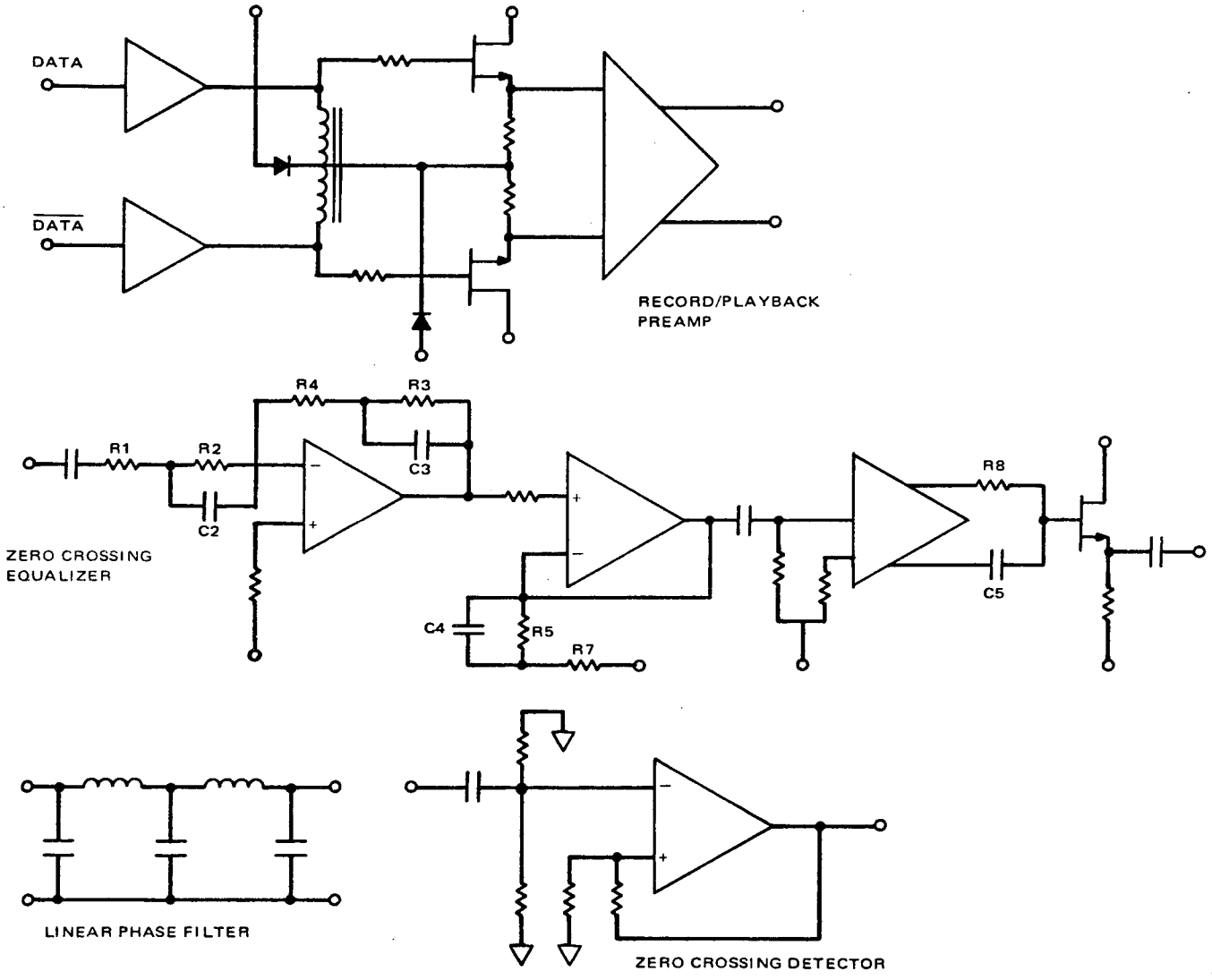

Figure 2-52. Equalizer and Filter Circuits

the data zero crossings. The cutoff frequency of the base-band filter will be set for 0.7 of the bit rate (308 kHz). The use of a passive type filter is dictated by minimum power consumption considerations, since 112 filters are required.

2.2.3.5 Zero-Crossing Detection for Tape Amplitude Dropout Protection

Zero-crossing detection will be used to restore the equalized playback signals into digital NRZ levels. The selected threshold point will depend upon the degree of play-back-signal degradation due to a non-ideal head-tape inter-face. The inherent inhomogeneity of magnetic tape (such as debris and nodules) will produce separation of the tape oxide from the head surface. This results in temporary losses of signal amplitude, commonly referred to as dropouts. Papers published by the Jet Propulsion Laboratory (JPL)[1] have attempted to classify dropouts with respect to width, length and density. Significant conclusions from these papers are:

(1) Tape cleaning reduces dropouts by several orders of magnitude
(2) Separation distances equal to or less than the track width is produced by small dropouts (left after tape cleaning).
(3) For small dropouts, the signal will degrade a maximum of -16 dB for a one-wavelength head-tape spacing.
(4) Dropout density (number of dropouts per unit length of tape) increases as the inverse cube of the effective wavelength.

The RCA HDRSS tape recorder operates at 0.24×10^6 flux reversals per meter of tape (0.12 Mb/m biphase). The wavelength at the

maximum-power point of the spectral density curve is 11μm (440 μinch). Individual track tape dropout measurements made at threshold levels of -40dB range from 0 to 30 individual dropouts (dropout length is not measured). The tape used is standard flight tape. That is, the tape is not machine cleaned, but it is wiped for 100 passes with cotton swabs prior to measurements.

The MCTR recorder will be operating at 0.8×10^6 flux reversals per meter. The wavelength at the maximum-power point of the spectral-density curve will be 3.4μm (135 μinch). This represents an increase of approximately three times the HDRSS recorder wavelength. Based on the JPL report, the dropout density per track, using the same tape and threshold level, should be expected to increase by a factor of nine over the HDRSS measurements. (If the length of the individual dropout is known, the anticipated bit error rate per track could be computed, based on the dropout density).

Based on the available data discussed and referenced above, a threshold level of -16dB should be adequate to compensate for small dropouts due to imperfections in tape. One wavelength for the MCTR is 3.4μm (135 μinch), which represents a "large" head-to-tape separation. An additional -6dB should be alloted for signal-amplitude variations due to tape tension changes in the drive (based on AED experience). Assuming a tape with only small dropouts and no additional debris, contamination, or oxide buildup, the ideal threshold level should be -22dB. This ideal condition can be obtained by machine-cleaning the tape as described in the referenced JPL report.

Figure 2-50 shows the circuitry selected for sensing zero crossing. Since equalization is first used to restore the zero crossings and to correct the waveshape, the method used for detection is not critical if the set threshold level is

above the noise level. The noise level from the linear-phase filter output is anticipated to be below -25 dB. Schmitt triggering with hysteresis was selected over analog-voltage limiting for two reasons. Integrated circuits are available that interface directly with the digital IC logic levels. Fast transition time for the NRZ-level changes, using a voltage limiter, are difficult at the higher frequencies of operation due to slew rate limitation of linear IC's.

2.3 System Hardware

2.3.1 Implementation of Digital Electronics

The hardware implementation of the record and playback digital electronics consists of various families of saturating logic. In general, where high speed is required, the TTL Schottky family was used; where the logic speed was slower, low power TTL or C-MOS logic was used to reduce the power requirements. The tables that follow list all of the circuit parts used, their types, the power dissipation per element, the total package count per circuit under consideration, and the total power required for the circuit. It should be noted that for the C-MOS family the power required by the logic element varies proportionally with the square of the frequency of the logic signal, so that in calculating the power dissipation for these elements the signal frequency or bit rates had to be considered. A 3:1 playback-record speed ratio was used for the estimate.

2.3.2 Mechanical Packaging of Digital Electronics Assembly

The MCTR digital data processing electronics packaging will incorporate six-layer boards with components mounted on both sides. The proposed board size is 173 mm (6.8 in.) by 140 mm (5.5 in.). Subtracting 13 square cm (2 sq. in.) for the connector mounting area leaves a usable area of approximately 230 sq. cm. (35 sq. in.) for each board side. The area to accomodate one flat pack on a six-layer board is 2.2 sq. cm (0.34 sq. in.). Using this technique, 100 flat packs can be mounted on each side of the board, for a packing density of 200 flat packs per board. Since the MCTR digital data-processing electronics requires approximately 1600 flat packs, the electronics container will require eight electronics boards and one harness

TABLE 2-7. PARAMETER COMPARISON OF PROPOSED LOGIC DEVICES

PARAMETER	TTL-STANDARD				TTL-HIGH				TTL-SHOTTKY				TTL-LOW POWER				COS/MOS INTEGRATER CIRCUITS			
	MIN	TYP	MAX	COND	MIN	TYP	MAX	COND	MIN	TYP	MAX	COND	MIN	TYP	MAX	COND	MIN	TYP	MAX	COND
tPLH (ns)	-	11	22	C_L=15pf R_L=400Ω	-	9	13	C_L-25pf R_L=300Ω	2	3	4.5	C_L=15pf R_L=280Ω	-	35	60	C_L=50pf R_L=4kΩ	-	-	110	C_L=50pf V_{DD}=5V
tPHL (ns)	-	7	15			65	10		2	3	5		-	31	60		-	-	75	C_L=50pf V_{DD}=5V
f Clock (MHz)	15	-	20		25	30	-		80	100	-		-	-	3		-	-	5	
I Sink (Ma)	16	-	-	V_{OH}=0.4V	-	20	-	V_{OH}=0.4V	-	20	-	V_{OH}=0.5V	-	-	1.8	V_{OH}=0.3V	-	-	0.5	V_{DD}=5V
Power Diss. (mW)	-	10	-	50% Duty Cycle	-	22	-	50% Duty Cycle	-	19	-	50% Duty Cycle	-	-	1.75	50% Duty Cycle	Frequency Dependent			

TABLE 2-8. CHIP ESTIMATE - SUMMARY

RECORD CKTRY	Pkgs.
Record Logic Clocks	16
BCH Encoder	28-1/4
Demultiplexing Logic	62
Double Density Encoders	73-1/2
	180

PLAYBACK CKTRY	Pkgs.
Double Density Decoders	243
Deskew Buffers	1016
Parallel-Serial Converters	113
Phase-Locked Loop - Rephasing Logic	52
	1424
Total Pkgs.	1604

board for interconnections. The board thickness is 1.57 mm (0.62 in.). Flat-pack height is approximately 2.54 mm (0.10 in.). The total board thickness required is therefore 6.65 mm (0.262 in.). Leaving room for tolerance, this yields approximately 7.6 mm (0.300 in.) per board. The total width required for eight boards would therefore be 61 mm (2.4 in.). Allowing additional width for board connectors and tolerance yields an approximate box width of 127mm (5.0 in.). Box height would be 173 mm (6.8 in.) plus 25 mm (1 in.) for the harness board, or approximately 200 mm (8 in.) for height. The box depth is 140 mm (5.5 in.) plus 12 mm (0.5 in.) for the mounting slides and wall thickness or approximately 152 mm (6.0 in.). The total box dimensions are therefore 127 mm (5 in.) x 200 mm (8 in.) x 152 mm (6 in.) or a total volume of 3.9 liters (240 cu. in.). Using a weight density of 0.97 kg/ℓ (0.035 lb/cu. in), the total box weight would be 3.8 kg (8.4 lb), or allowing for margin, 4.1 kg (9 lb.).

2.3.3 MCTR Power Budget

2.3.3.1 Summary

	WATTS				
			PB		
TRANSPORT	STANDBY	REC	FAST	SLOW	REWIND
Servo Control	--	1.00	1.00	1.00	1.00
DC Mag. Erase	--	0.50	--	--	--
EOT & TLM	0.25	0.25	0.30	0.30	0.30
Encoder Elec.	--	0.70	0.70	0.70	0.70
Motor Driver	--	2.94	6.80	2.94	6.80
Record Amps	--	9.70	--	--	--
"PB" Buffer	--	--	4.00	4.00	--
"PB" Amp/Equalizers	--	--	48.00	48.00	--
Limiters	--	--	14.50	14.50	--
Servo Clock "PB" Amp	--	--	0.50	0.50	--
DIGITAL PROCESSING ELECTRONICS	--	14.36	30.34	not est.	--
TOTAL	0.25	29.45	106.94		8.80

	TIME MINUTES	POWER WATTS	ENERGY WATT HOURS
Record	30	29.4	14.7
Rewind	10	8.8	1.47
Playback	10	106.94	17.82
Standby	50	0.25	0.25
Total	100	20.5 Avg.	34.24

Thus, the average power for a typical 100-minute orbit will be 20.5 watts.

2.3.3.2 Motor Power Calculations

Negator System - 2.4N differential tension

Tape Speed = 1.73m/s read fast; 0.575 m/s read slow and write

Capstan Dia. = 15mm

Motor Constants:

KT = 0.0642 N·m/A

KB = 63.5 mv/rad/sec

R = 9Ω/winding

Capstan Torque = $2.4\ N \cdot 7.5 \cdot 10^{-3} m = 0.018\ N \cdot m$

Current = $0.018\ N \cdot m \cdot 0.0642\ \frac{N \cdot m}{A} = 0.28A$

Capstan Speed, read, fast = $\frac{1.73\ m/sec}{7.5 \cdot 10^{-3} m/rad} = 231\ \frac{rad}{sec}$

read, slow/write = $\frac{0.575\ m/sec}{7.5 \cdot 10^{-3} m/rad} = 77\ \frac{rad}{sec}$

Back EMF, read, fast

$= 6.35 \cdot 10^{-2}\ \frac{V}{rad/sec} \cdot 231\ \frac{rad}{sec} = 14.7V$

read slow/write $= 6.35 \cdot 10^{-2} \frac{V}{rad/sec} \cdot 77 \frac{rad}{sec} = 4.9V$

IR Drop = $9\Omega \cdot 0.28A = 2.5V$

Total Voltage, read, fast = 14.7 + 2.5 = 17.2V

read slow/write = 4.9 + 2.5 = 7.4V

Mech. Power, read, fast $= 0.018\ N \cdot m \cdot 231 \frac{rad}{sec} = 4.17W$

read, slow/write $= 0.018\ N \cdot m \cdot 77 \frac{rad}{sec} = 1.39W$

Elec. Power read, fast = $17.2V \cdot 0.28A = 4.82W$

to Motor

read, slow/write = $7.4V \cdot 0.28A = 2.07W$

Motor Efficiency, read, fast $= \frac{4.17W}{4.82W} \times 100 = 86.4\%$

read, slow/write $= \frac{1.39W}{2.07W} \times 100 = 67.2\%$

Current @23V, read, fast $= \frac{4.82W}{23V} = 0.209A$

(24.5V-VCE)

read, slow/write $= \frac{2.07W}{23W} = 0.09A$

Current w/33%, read, fast = $1.33 \cdot 0.209A = 0.278A$

margin read, slow/write = $1.33 \cdot 0.09A = 0.120A$

Total Elec. Power, read, fast $= \frac{24.5V}{23V} \cdot 4.82W = 5.13W$

read, slow/write $= \frac{24.5V}{23V} \cdot 2.07W = 2.2W$

Efficiency @24.5V, read, fast $= \frac{4.17W}{5.13W} \times 100 = 81.2\%$

$$\text{read, slow/write} = \frac{1.39W}{2.2W} \times 100 = 63.2\%$$

Total Elec. Power, read, fast = $1.33 \cdot 5.13W = 6.83W$

w/33% margin read, slow/write = $1.33 \cdot 2.2W = 2.93W$

Efficiency @ 24.5V, read, fast = $\frac{4.17W}{6.83W} \times 100 = 81\%$

W/33% margin

$$\text{read, slow/write} = \frac{1.39W}{2.93W} \times 100 = 47.4\%$$

2.3.3.3 Electronics Power Estimates

2.3.3.3.a Detailed Digital Electronics

RECORD POWER

Qty.	(BCH Encoder & Demux) Clocks	Pd/Ckt, mW	Pkgs.	Total Power - W
7	÷13 ctr (7 TTLS F/F)	160	3-1/2	1.120
8	÷13 Decode Quad NAND-TTLS	20	4	0.160
4	2 input NAND-TTLS	20	1	0.080
4	÷7 ctr F/F-TTLS	160	2	0.480
1	Flip-Flop (F/F-TTLS)	160	1/2	0.160
2	3 input AND gates TTLS	30	2/3	0.060
2	2 input NAND gates TTLS	20	1/2	0.040
	6.14 MHz clocks			
3	2 input NAND gates TTLS	20	3/4	0.060
2	4 input NAND gates TTLS	20	1	0.040
8	Inverter TTLS	20	2	0.160
	SUBTOTAL		≈16	2.48W
	BCH Encoder			
8	F/F (Register BCH_A) TTLS	160	4	1.280
8	2-input N.G. (Register BCH_A) TTLS	20	2	0.160
1	8-input N.G. (Register BCH_A) TTLS	20	≈1/2	0.020
8	3 input A.G. (Timing for Readout) TTLS	30	2-2/3	0.240

RECORD POWER (Continued)

Qty.	BCH Encoder (Continued)	Pd/Ckt, mW	Pkgs.	Total Power - W
3	F/F (Sync ÷8) TTLS	160	1-1/2	0.480
1	N.G. 2 input (Sync ÷8) TTLS	20	1/4	0.020
2	Inverter (Sync ÷ 8) TTLS	20	1/3	0.040
8	4 input N.G. (BCH_A readin) TTLS	20	4	0.160
3	F/F (Sync ÷ 8) TTLS	160	1-1/2	0.480
1	2 input N.G. (Sync ÷ 8) TTLS	20	1/4	0.020
2	Inverter (Sync ÷ 8) TTLS	40	1/3	0.040
7	F/F (BCH_B) TTLS	160	3 1/2	1.120
21	3 input N.G. (exc. or)TTLS	20	7	0.420
3	3 input N.G. (read out) TTLS	20	1	0.060
3	2 input N.G. (read out) TTLS	20	3/4	0.060
	SUBTOTAL		28-1/4	5.600
	Demultiplexing Logic			
7	D type FF (TTLS) Buffer 1	160	3-1/2	1.12
14	D type FF (TTLS) Buffer 2	160	7	2.24
14	Level Converters (SN5476) Buffer 2	40	3-1/2	0.560
14	Pull-up Resistors (1K) 50% Duty Cycle)	12.5	-	0.175
28	8 bit Dynamic Shift Register (CD40151) Buffer 3	80	28	2.44
20	Divide by N Counter (Used as Static Storage Register) 98 bits CD-4018A)	3.5	20	0.070
	SUBTOTAL		62	6.6 watts
	Double Density Encoders			
98	AND-OR Select Ckts (exc.-OR) C-MOS (CD-4019A)	2.5mw	24-1/2	0.245
98	FF C-MOS (CD-4013A)	0.3mw	49	0.029
	SUBTOTAL		73-1/2	0.277

2.3.3.3.b Playback Power Estimate

DENSITY DECODERS

Qty.			Power Each - mW	Pkgs.	Rate ~1.3 MHz Total Power, mW
2	F/F	(CD-4013A)	0.8	1	1.6
6	2 input gates	CD-4011D	1.0	1-1/2	6.0
6	Inverter	CD-4009A	4.0	1	24.0
2	4 input gates	CD-4012D	1.0	1	2.0
		SUBTOTAL		3-1/2	33.6 mW/track
		98 ckts of above		243 pkgs.	3.29 watts

DESKEW BUFFER

Qty.	Cktry	Diss/Ckt mW	Pkgs.	Total Power, Watts
7	MOD 8 Counter & Decode (COS MOS CD 4022A)	20	7	0.140
784	Read in AND gates (2 input) Quad CD 4011A	0.1	196	0.0784
784	Flip Flops (Storage) CD 4013A	0.7	392	0.548
784	Readout NAND gates (2 input) CD 4011A	0.1	196	0.0784
98	Readout 8 input NAND gates SN 54L30	1.37	98	0.134
98	2 input AND gates SN 54L00	1.75	25	0.171
1	MOD 8 system CTR & Decode CD 4022A	20	1	0.020
4	4 bit delay F/F CD 4013A	0.7	2	0.003
1	Delay 2 F/F CD 4013A	0.7	1	-
784	CMOS/TTL Buf (HCX) CD 4010A	6	98	4.700
	SUBTOTAL		1016	5.8728

PARALLEL-SERIAL CONVERTER

Qty.			Diss/Ckt mW	Pkgs.	Total Power - W
98	F/F shift registers	TTLS	160	49	15.68
8	F/F ÷49 Johnson ctr	TTLS	160	4	0.64
35	Buffers F/F/3 (SN 54504)	TTLS	20	6-1/6	0.70
7	Buffers (SN 54504)	TTLS	20	1-1/6	0.14
98	2-input gates (Parallel transfer) TTLS		20	24-1/2	1.96
6	Dual guads	TTLS	20	25	0.12
2	F/F (Timing Logic)	TTLS	160	1	0.32
10	2 input gates (gating logic) TTLS		20	2-1/2	0.20
	SUBTOTAL			113-1/3	19.76

PHASED-LOCKED LOOP

Qty.		Diss/Ckt mW	Pkgs.	Total Power - W
14	Delay Ckt and FW Rect (Hybrid)	50	14	0.700
7	Phase detectors and charge pump ½ IC and 1 hybrid	30	7 hybrid 4 IC	0.210
7	VCM (MC4324F - typical)	90	7	0.630
7	F/F (COS MOS - clock cktry)	60	4	0.420
7	2 input N.G. (COS MOS - clock cktry)	40	4	0.280
7	2 F/F (LP-TTL) Rephasing logic	8	7	0.112
7	6 gates (LP-TTL) Rephasing logic	1.75	≈5	0.074
	SUBTOTAL		52 pkgs.	2.426

2.3.3.3.c Digital Signal Processing Power Estimate

Summary

Record	Watts
Record Logic Clocks	2.48
BCH Encoder	5.60
Demultiplexing Logic	6.60
Double Density Encoders	0.28
TOTAL	14.96

Playback (High Speed)	
Double Density Decoders	3.29
Buffers	5.87
Parallel/Serial Converters	18.76
Phase Locked Loop and Rephasing Logic	2.42
TOTAL	30.34

2.3.4 Weight Budget

2.3.4.1 Primary Tape Transport

Transport	Weight Kg.	Lb.
Reels	2.17	4.77
Tape	2.70	5.94
Motor	0.91	2.00
Negator Syst.	3.77	8.30
Idlers	0.34	0.75
Heads & Mounts	0.57	1.25
Pinch Rollers	0.46	1.00
Chassis	5.67	12.50
Flywheel	0.68	1.50
Enclosure	5.90	13.00
Electronics	4.10	9.00
TOTAL	27.26	60.00

2.3.4.2 Alternate Tape Transport

	Weight	
	Kg.	LB.
Reels & Motors (2)	4.00	8.77
Tape	2.70	5.95
Idlers	0.34	0.75
Heads & Mounts	0.57	1.25
Pinch Rollers	0.46	1.00
Chassis	5.67	12.50
Enclosure	5.90	13.00
Electronics	4.10	9.00
(No Flywheels)	23.72	52.21

2.3.5 Reliability Aspects

A Failure Modes, Effects, and Criticality Analysis will be performed for each electrical component in the MCTR showing failure modes, possible causes, symptons and local effects, compensatory provisions, level of severity, failure probability, and effect upon the mission. In addition, other provisions of the reliability program include 100-percent preconditioned parts to eliminate infant mortality, and traceability to allow exclusion of all affected parts if a batch problem exists.

Several major electrical failure modes have been eliminated by the proposed use of brushless-versus-brush motors and by the incorporation of optical end-of-tape sensors rather than contactor bars or microswitches, both of which incorporate physical contact with the tape.

The clock signal, used as the motor-drive servo reference during playback mode, will be derived from the previously recorded digital data clock channels in the Digital Data Processor, using two clock channels for redundancy.

2.4 Ground Station

2.4.1 General

The multichannel tape recorder ground station is configured to extract the spacecraft sensor signals from the down link signal for operation either during stored-mode reception or during direct real-time mode reception. The two modes of operation share all signal processing components except for stored-mode operation, which requires a parallel-to-serial converter to convert the four-phase data to NRZ. The multitrack tape recorder ground terminal block diagram is shown in Figure 2-53. The stored-mode reception occurs at 129.16 Mb/s and the real-time mode reception occurs at 39.9 Mb/s.

A directive antenna and cooled preamplifier receive the down-link signal with a system noise temperature of 200^{o}K, assuming 14 GHz and a 5-degree elevation angle.

2.4.2 Ground Station Operation During Stored-Mode Reception

The stored-mode signal, subsequent to receiver processing, emerges from the if. amplifier and is further processed by: (1) four phase demodulator, (2) stored mode timing extractor, (3) parallel-to-serial converter, (4) BCH error corrector, (5) sensor data demultiplexer and the sub-channel demultiplexer, and (6) the digital-to-analog converters which reproduce the sensor data. (The numbers in parentheses refer to the block numbers in Figure 2-53).

The multichannel tape recorder ground station, during stored-mode reception, has the following operational highlights:

- The if. signal from the receiver is processed by the four-phase demodulator, which yields two 64.58 Mb/s NRZ streams. The stored-mode timing extractor provides bit and frame timing signals.

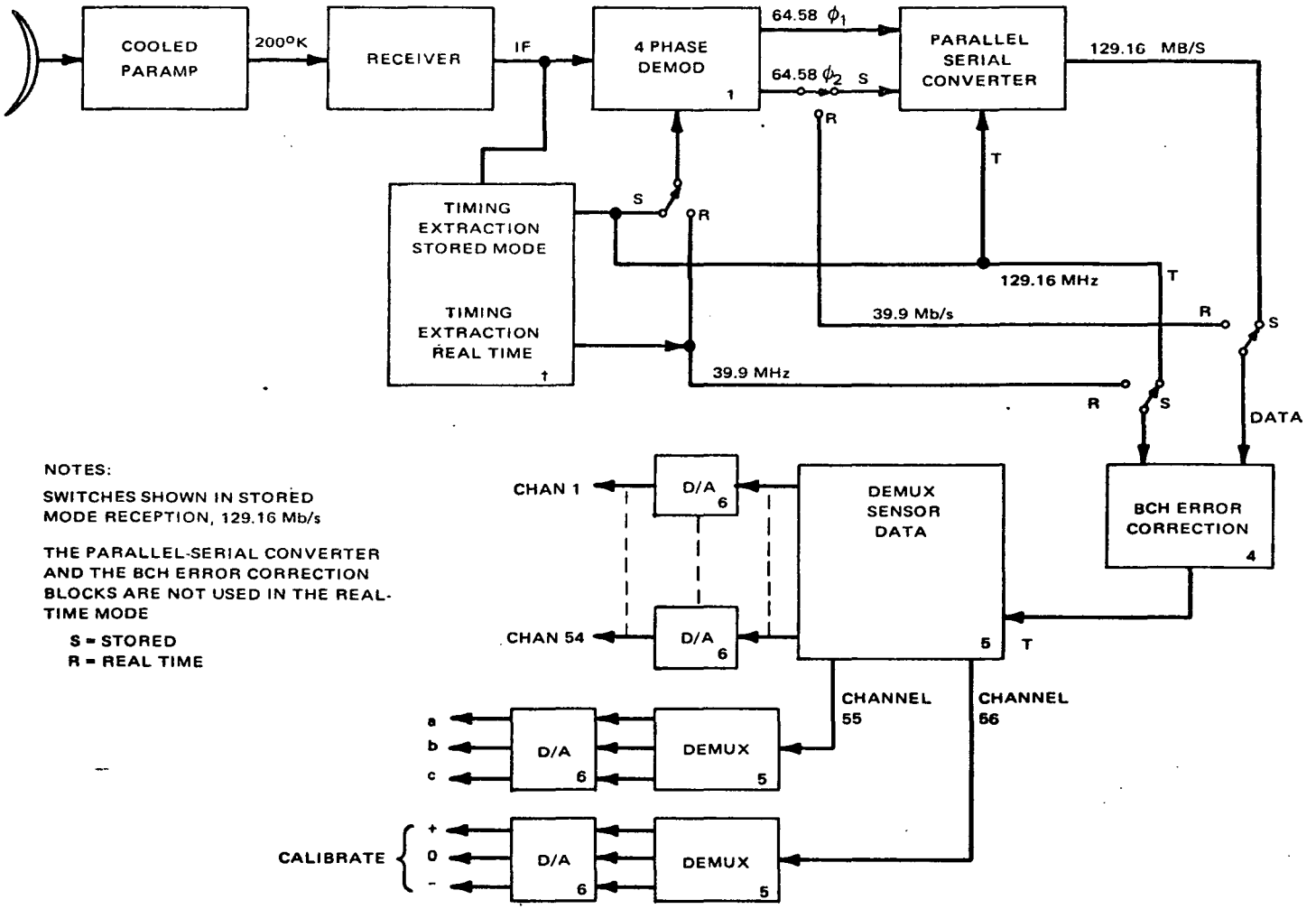

Figure 2-53. MCTR Ground Terminal, Block Diagram

- The two 64.58-Mb/s NRZ streams feed a parallel-to-serial converter, resulting in a 129.16-Mb/s stream.

- The data stream goes to a BCH error corrector, resulting in corrected NRZ stream representing multiplexed sensor data.

- The sensor data, which has been error corrected, is now demultiplexed into sensor channels 1 through 55, and calibrate channel 56.

- The parallel data is digital-to-analog converted to yield sensor channels 1 through 55 and calibrate channel 56.

- Channel 55 is demultiplexed and then digital-to-analog converted to reconstruct analog data a, b, and c.

- Channel 56 is demultiplexed and then digital-to-analog converted to reconstruct calibrate analog data.

2.4.3 Ground-Station Operation During Direct Real-Time Mode Operation.

The direct real-time mode signal, subsequent to receiver processing, emerges from the if. amplifier and is further processed by: (1) a four-phase demodulator, (2) a direct real-time mode timing extractor, (5) a sensor data demultiplexer and the sub-channel demultiplexers, and (6) the digital-to-analog converters which yield approximations to the sensor data. (Numbers in parentheses refer to block numbers in Figure 2-53).

The multi-channel tape recorder ground station, during direct real-time mode reception, has the following operational highlights.

- The if. signal from the receiver is processed by the four-phase demodulator, which yields a 39.9 Mb/s NRZ stream. The real-time mode timing extractor provides bit and frame timing signals.

- The data stream is now demultiplexed into sensor channels 1 through 55, and calibrate channel 56.

- The parallel data is digital-to-analog converted to yield sensor channels 1 through 55 and calibrate channel 56.

- Channel 55 is demultiplexed and then digital-to-analog converted to reconstruct analog data a, b, and c.

- Channel 56 is demultiplexed and then digital-to-analog converted to reconstruct calibrate analog data.

2.5 Link Calculations

2.5.1 General

The link requirements and parameters with main features as shown below are calculated for: (1) stored-mode operation and (2) the direct real-time mode of operation.

These parameters and requirements are:

- Information rate
- Transmitter modulation
- Keying rate
- Carrier-to-noise density ratio
- Bit error rate
- Center frequency, noise temperature, and elevation angle
- Required received power

2.5.2 Stored Playback Mode

During stored-mode operation, a four-phase PM transmitter is modulated at an information rate of 129.16 Mb/s. The symbol rate is 64.58 million symbols per second, as a result of encoding two-level NRZ to four phases. The spectrum of a PM transmitter modulated by a signal with a symbol rate of 64.58 million symbols per second is 64.58 MHz each side of the carrier frequency. This yields a minimum required rf bandwidth of 129.16 MHz.

The link calculations for stored-mode operation are:

- Information rate 129.16 Mb/s
- Four-phase PM transmitter
- Symbol rate, 64.58 million symbols per second

Minimum rf band required: 129.16 MHz

$$\frac{E_s}{N_o} = 12.6 + 1.4 = 14 \text{ dB} \quad Pe = 10^{-5}$$

Keying rate 64.58 M baud 78.10 dB

$$\frac{C}{N_o} = 92.10 \text{ dB} \quad Pe = 10^{-5}*$$

*Add 0.94 dB $Pe = 10^{-6}$

" 1.68 dB $Pe = 10^{-7}$

" 2.4 dB $Pe = 10^{-8}$

Required received power = $228.6 + 10 \log T + \frac{C}{No}$ (dBW)

Add circuit margin required.

At 14 GHz minimum T $\approx$ 200^{o}K at 14 GHz, 5^{o} elevation angle.

10 log 200 = 23 dB

$P_r = -205.6 + \frac{C}{N_o} = -205.6 + 92.10 + 0.94 = 112.27$ dBW for Pe = 10^{-6}

Add margin.

2.5.3 Direct Real-Time Mode

During the direct real-time mode operation, a biphase transmitter is modulated at an information rate of 39.9 Mb/s. The symbol rate is 39.9 million symbols per second, as a result of encoding two-level NRZ to two phases.

The link calculations for direct real-time operation are:

Information Rate: 39.93 Mb/s
Use biphase $\pm 90^{o}$

Available rf band: 133 MHz

E/N_o = 9.6 + 1 = 10.6 dB Pe = 10^{-5}

Keying Rate: 39.93 M-Baud = 74.0 dB

(NOTE: Bandwidth = keying rate for signal associated with E)

C/N_o = 84.6 dB Pe = 10^{-5*}

B = 133 MHz = -81.25 dB (Note: This is noise bandwidth)

C/N_o 3.35 dB Pe = 10^{-5*}

Required received power = $kT(C/N_o)$

Where

k = Boltzman's constant, joules/^{o}K

T = degrees Kelvin

(C/N_o) = watts/(watts/sec^{-1}) = sec^{-1}

At 14 GHz, minimum T = 200^{o}K at 5^{o} elevation angle.

$10 \log_{10} 200 = 23$ dB

Required received power (playback mode) = Pr

$$= -228.6 + \log_{10} T + 10 \log_{10} C/N_o$$

$$Pr = -228.6 + 23 + 84.6 + 0.94 = 120.06 \text{ dBW} \quad \text{at Pe} = 10^{-6}$$

*Add: 0.94 dB, Pe = 10^{-6}

1.68 dB, Pe = 10^{-7}

2.4 dB, Pe = 10^{-8}

Add circuit margin.

2.5.4 MTR Link Specification

2.5.4.1 Stored Mode

Information rate 133 Mb/s
Four Phase PM transmitter
Symbol rate 66.5 million symbols per second.

Minimum rf band required, 133 MHz

$$\frac{E_s}{N_o} = 12.6 + 1.4 = 14 \text{ dB} \qquad Pe = 10^{-5}$$

Keying rate 66.5 M-baud 78.23 dB

$\frac{C}{N_o}$ = 92.23 dB Pe = 10^{-5}*

B = 81.25 dB

$\frac{C}{N}$ = 11 dB Pe = 10^{-5}*

*Add 0.94 dB Pe = 10^{-6}
" 1.68 dB Pe = 10^{-7}
" 2.4 dB Pe = 10^{-8}

Required received power = $-228.6 + 10 \log T + \frac{C}{N_o}$ (dBW)

add circuit margin required.

At 14 GHz minimum T ≈ 200°K at 14 GHz, 5° elevation angle

10 log 200 = 23 dB

$P_r = -205.6 + \frac{C}{N_o} = -205.6 + 92.23 + 0.94 = -112.4$ dBW for Pe = 10^{-6}

Add margin.

2.5.4.2 Direct Real-Time Mode

Information rate 43 Mb/s
Use biphase ±90°
Available rf band 133 MHz

$\frac{E}{N_o} = 9.6 + 1 = 10.6$ dB Pe = 10^{-5}

Keying rate 43 M-baud 76.38 dB

$$\frac{C}{N_o} = 86.98 \text{ dB} \quad Pe = 10^{-5*}$$

B = 133 MHz 81.25 dB

$$\frac{C}{N} = 5.73 \text{ dB} \quad Pe = 10^{-5*}$$

*Add 0.94 dB, Pe = 10^{-6}
" 1.68 dB, Pe = 10^{-7}
" 2.4 dB, Pe = 10^{-8}

Required received power = $-228.6 + 10 \log T + \frac{C}{N_o}$ dBW and add required circuit margin.

$$Pr = -205.6 + \frac{C}{N_o} = -205.6 + 86.98 + 0.94 = -117.7 \text{ dBW} \quad Pe = 10^{-6}$$

Add margin.

3.0 SYSTEM STUDIES AND TRADEOFFS

3.1 Analog-Digital System Comparison

In the analog approach, each sensor baseband frequency-modulates a VCO and the FM signals are recorded on separate tape-recorder tracks. If sensors have different bandwidths, tape speed must be high enough to accommodate the widest baseband.

The multi-channel playback signal may be transmitted to ground by using frequency-division multiplex, or by digitizing and time-division multiplex. Frequency-division multiplex is undesirable for a large number of channels because of the linearity requirement and the excessive bandwidth requirement. For the case of 54 sensor channels with 40 kHz basebands and a 3:1 playback speed-up, it is better to convert to a serial PCM stream, which can modulate a four-phase PM transmitter. For example, FDM-FM requires a band of about 570 MHz, depending on down-link margin, whereas PCM requires a band of only 120 MHz. Time-base error correction can be done on the ground by including several flutter channels in the multiplexed down-link signal.

In the digital approach, each sensor baseband is sampled and digitized into a PCM signal. The PCM signals are time-division multiplexed into a serial stream for either recording or real-time transmission, as desired.

For recording, the serial digital signal is converted to many parallel channels. On playback, these parallel digital channels are converted to serial form for transmission to ground. For the same case of 57 sensor channels, 98 data-record channels are required to permit 30 minutes of record time.

In the digital system, it is a requirement to remove time-base error and skew to permit parallel-to-serial conversion in the playback mode. Thus, there is no recorder time-base error in the ground received signal. In the digital approach, extra bits can be added to provide error correction on the ground. This permits correction of all non-overlapping burst errors caused by dropouts in the parallel channels. It also permits complete loss of a single channel if encoding provides for one error correction in 98 bits, or complete loss of two channels if encoding provides for two error corrections in 98 bits of information and double error correction gives 85 bits of information out of a total of 98 bits.

3.2 Analog-Digital Performance Comparison

Comparing analog and digital approaches, the following items are evident:

Analog	Digital
64 Recorder tracks	112 Recorder tracks
Crosstalk between channels requires high modulation index, increased band, and increased tape speed, giving nearly the same tape speed as for digital.	Crosstalk not a problem with digital recording. Better immunity to noise and crosstalk.
790 m (1930 ft) of tape, 0.33 m/s (13 in./s).	1040m (3400 ft) of tape, 0.577 m/s (22.7 in./s)
Time-base error not fully correctable. Registration in multispectral scanner is difficult.	No time-base error and no multispectral registration problems.
Accuracy limited to 1%.	Accuracy determined by number of bits in PCM word encoding.
Recorder channels not all oprating with the same efficiency.	All recorder channels operating at same efficiency.
Playback signals must be digitized and put in serial form for down-link transmission.	Playback signals are already digitized but must be put in serial form.

Analog	Digital
Loss of a record channel not easily correctable.	Encoding provides error correction to recover a lost channel (see Para. 3.2.1).
Tape dropouts are not correctable.	Non-overlapping dropouts and most random errors are corrected.
System parameters are dependent on input sensors.	Universal storage system for future applications.

3.2.1 Encoding for Data Correction

The BCH code[2] for one error correction is the same as the Hamming code[3]. The code used is (127, 120, 1), where the word is 127 bits with 120 data bits, 7 parity bits, and the capability to correct one error. The enclosed chart (Figure 3-1) is extracted from data from Reference 3, where $P_{E_{BEFORE}}$ and $P_{E_{AFTER}}$ are respectively the bit error rates before and after correction of one random error. If data from one spacecraft tape track is lost, the ground station decoder will provide the missing data.

3.3 Comparison of Coplanar and Coaxial Reel Configurations

In the trade-off analysis between the coplanar and coaxial arrangement for the tape reels, it was the tape width and length to be handled that determined the final configuration. 1100 meters of 50.8-mm-wide tape weighs approximately 2.70 kg. To support this weight during environmental vibration would require a much heavier structure in a coaxial arrangement than that for a coplanar design, where the reels are independently mounted close to the supporting chassis.

In a coaxial arrangement, it is necessary to twist the tape at some point or points in order to effect the transition from

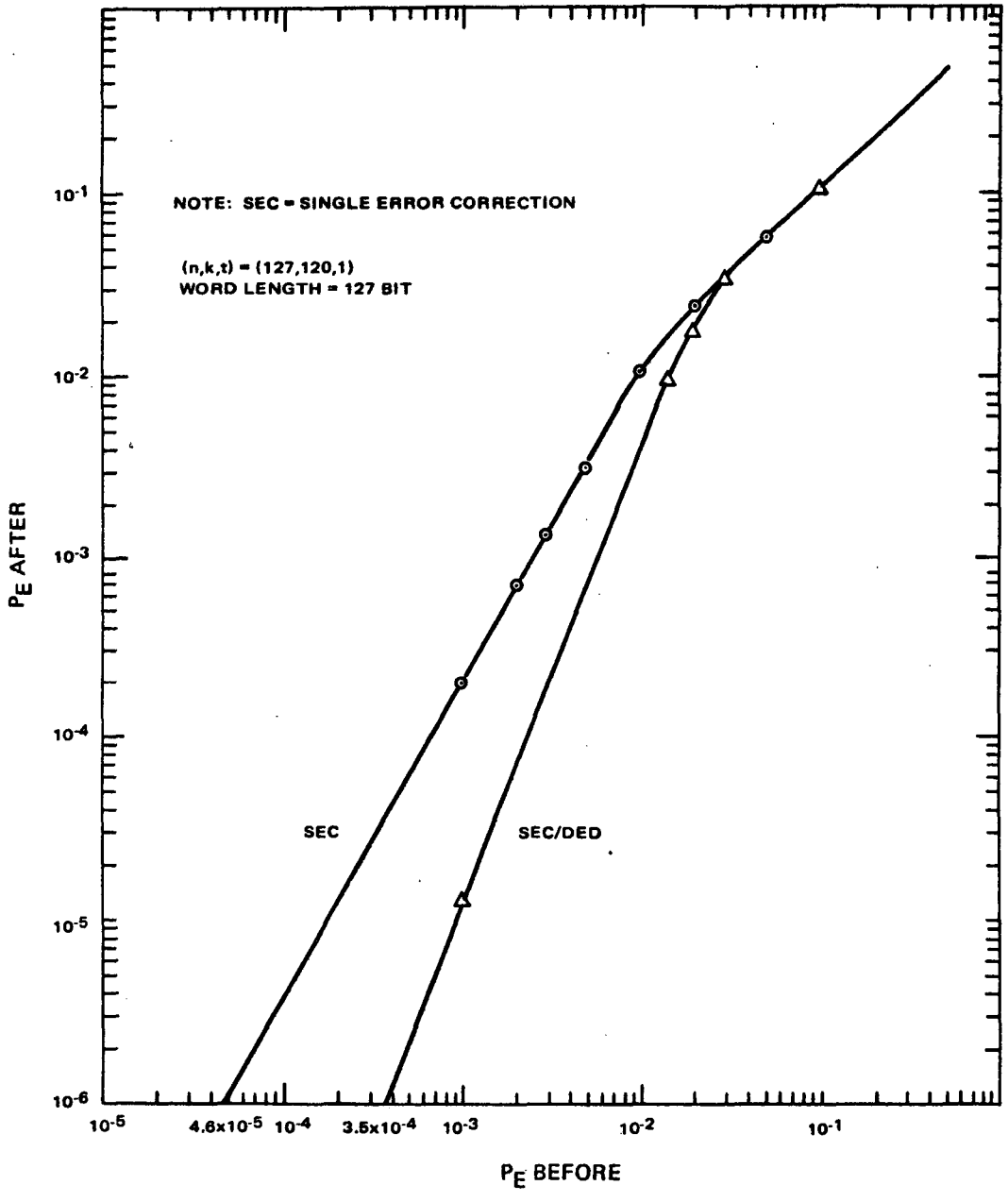

Figure 3-1. Bit Error Rate After Correction of One Error for BCH Code (127, 120, 1).

one level to the other. This could introduce problems in tape tracking and tensioning, requiring the probable use of crowned idlers and, certainly, heavier negator springs in order to provide the increased tape tension to ensure proper tracking control. Experience has shown that the tape tension can be as little as 2.5 Newtons for 50.8-mm-wide tape on a coplanar transport, but could be as high as 8.5 Newtons on a coaxial transport.

There is a possible advantage to the coaxial arrangement in that its footprint on the spacecraft could be smaller than that for the coplanar. The coaxial system would, however, be considerably higher in profile.

The coplanar arrangement was therefore selected, since it offered reduced weight and complexity over that anticipated for a coaxial arrangement.

3.4 Sensor Analog-to-Digital Conversion Studies

3.4.1 Introduction

Prior to termination of the analog-to-digital-conversion studies, criteria were established in accordance with Reference 4 for the selection of sampling rates of sensor data and pre-sampling filter parameters. The numerical results are as shown in Table 3-1. The sensor spectrum has a (sinx/x) form, which suggests the use of the first zero of the sensor power density response as a normalization factor for the relative sampling rate f_s/f_o. Asterisks are next to relative sampling rates in the table that yield less than one-percent-rms interpolation error for the case described in the next subsection. The following discussion shows the equations used in a computer program that allows variation of sampling rate, pre-sampling-filter cutoff frequency, and filter cutoff rate for resultant percentage of rms error, based on the use of the optimum interpolation error.

3.4.2 Discussion

Following Downing[4], Page 146; equation (7.29) is substituted into equation (7.27) to yield the minimum interpolation error power.

$$P\varepsilon_{min} \cong \int_{o}^{\infty} \frac{G_m(f)\ \ G_m\ (f-f_s)\ df}{G_m(f) + G_m(f-f_s}$$

Where $G_m(f)$ is the power spectral density from the sensor source including the weighting factor associated with the sensor (pre-sampling) aliasing filter.

We again follow Downing, Page 146, equation (7.28) by weighting the sensor power spectrum density by the magnitude squared Butterworth response. This will permit the development of a functional relationship between minimum interpolation error, filter break frequency and filter cutoff rate.

Therefore:

$$G_m(f) = \left\{ \frac{\sin\left[\frac{\pi f}{f_o}\right]}{\left[\frac{\pi f}{f_o}\right]} \right\}^2 \left\{ \frac{1}{1 + \left(\frac{f}{f_c}\right)\ 2k} \right\}$$

where: f_o is the frequency where the first zero of the sensor power density response occurs.

and: f_c is the frequency where the filter response is 3 dB below reference; and is defined as the filter bandwidth.

and: 6k dB/octave is the filter cutoff rate.

The symbols used in the program are as follows:

A = Lower limit of integration

B = Upper limit of integration

N = Number of points for numerical integration

Y = Sampling frequency, (f_s)

C = Frequency where Butterworth response is down 3 dB, (f_c)

K = k where aliasing filter rolls off at 6k dB/octave.

M = Normalizing factor, set equal to sensor output power. This normalizes $P\varepsilon_{min}$ to yield % RMS error.

F = Result

The results of typical calculations are listed in Table 3-1.

TABLE 3-1. NUMERICAL RESULTS

$\frac{f_s}{f_o} = \frac{\text{sampling rate}}{\left[\text{1st zero of sensor power density response}\right]}$	% RMS Error	Comments
2.00	3.74	k = 1 so that aliasing filter has 6 dB/ octave skirt.
2.50	1.65	
2.75	1.42	
3.00	1.45	C = 1 so that aliasing filter bandwidth corresponds to the 1st zero of sensor power density response.
3.10	1.24	
*3.25	0.84 < 1%	
*3.50	0.67 < 1%	
2.00	1.54	K = 1 so that aliasing filter has 6 dB/ octave skirt.
*2.25	0.89 < 1%	
*2.50	0.63 < 1%	
		C = 0.5 so that aliasing filter bandwidth is one-half the sensor bandwidth.

4.0 LIST OF REFERENCES

1. W.Van Keuren, An Examination of Dropouts Occurring in the Magnetic Recording and Reproduction Process, Jet Propulsion Laboratory.

2. R. W. Lucky et al, Principles of Data Communications, New York, McGraw-Hill Book Co., 1968.

3. R. G. Marquart and J. C. Hancock, "Performance of Hamming Codes," IEEE Transactions on Space Electronics and Telemetry, December 1966, pp. 115 - 126.

4. J.J. Downing, Modulation Systems and Noise, Prentice-Hall, 1964.

5.0 NEW TECHNOLOGY

New Technology reporting requirements are covered by separate reports in compliance with the needs of the NASA Technology Utilization Officer, the NASA Patent Counsel, and the NASA New Technology Clause.

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APPENDIXES

NOTE: All appendixes (A through L) are located in Volume II of this report. However, for the reader's convenience, Appendixes D and G are included in this volume.

APPENDIX D

CIRCUIT ANALOGUES OF MECHANICAL SYSTEMS, BASED UPON DIMENSIONAL ANALYSIS

APPENDIX D

CIRCUIT ANALOGS OF MECHANICAL SYSTEMS
(BASED UPON DIMENSIONAL ANALYSIS)

I. Magnetic Model (Vs) = (NΦ) or Weber turn (flux linkage) factored.

$$V = (Vs)\cdot\frac{1}{s} \equiv (Vs)\cdot\frac{rad}{s}\ , \quad \text{Voltage} \equiv \text{Velocity x (Vs)}$$

$$A = \frac{W}{V} = \frac{J}{(Vs)} = \frac{Nm}{(Vs)}\ , \quad \text{Current} \equiv \text{Torque/(Vs)}$$

$$\Omega = \frac{V}{A} = \frac{V^2}{W} = \frac{V^2 s}{J} = (Vs)^2\cdot\frac{1}{Js} = \frac{(Vs)^2}{Nm/1/s}\ ,\ \frac{(Vs)^2}{Nm/rad/s}$$

$$\text{Resistance} \equiv \frac{(Vs)^2}{\text{Torque/Velocity}}$$

$$H = \frac{Vs}{A} = \frac{V^2 s}{W} = \frac{(Vs)^2}{J} = \frac{(Vs)^2}{Nm} \equiv \frac{(Vs)^2}{Nm/rad}\ ,$$

$$\text{Inductance} \equiv \frac{(Vs)^2}{\text{Torque/radian}}$$

$$F = \frac{As}{V} = \frac{Ws}{V^2} = \frac{J}{V^2} = \frac{Nm.s^2}{(Vs)^2} = \frac{kgm^2}{(Vs)^2}\ , \quad \text{Capacitance} \equiv \frac{\text{Inertia}}{(Vs)^2}$$

II. Electric Model (As) or coulomb factored

$$V = \frac{W}{A} = \frac{J}{(As)} = \frac{Nm}{(As)}\ , \quad \text{Voltage} \equiv \text{Torque/(As)}$$

$$A = \frac{(As)}{S} \equiv (As).\frac{rad}{S}\ , \quad \text{Current} \equiv \text{Velocity x (As)}$$

$$\Omega = \frac{V}{A} = \frac{W}{A^2} = \frac{J}{A^2 s} = \frac{1}{(As)^2}\cdot\frac{Nm}{1/s} \equiv \frac{Nm/rad/s}{(As)^2}\ ,$$

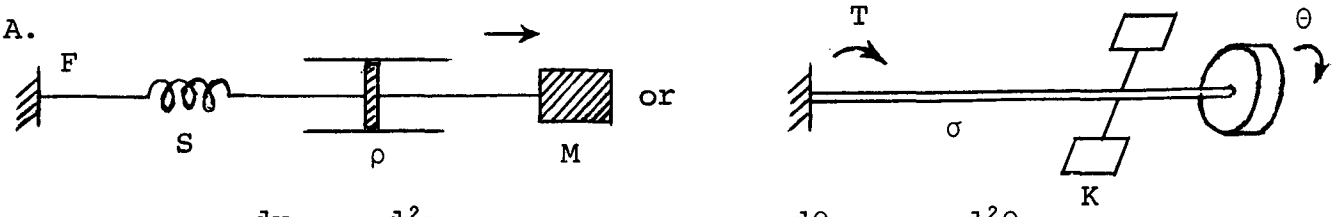
$$\text{Resistance} \equiv \frac{\text{Torque/Velocity}}{(As)^2}$$

$$H = \frac{Vs}{A} = \frac{Ws}{A^2} = \frac{J}{A^2} = \frac{Nm.s^2}{(As)^2} = \frac{kgm^2}{(As)^2}, \quad \text{Inductance} \equiv \frac{\text{Inertia}}{(As)^2}$$

$$F = \frac{As}{V} = \frac{A^2 s}{W} = \frac{(As)^2}{J} = \frac{(As)^2}{Nm} \equiv \frac{(As)^2}{Nm/rad}, \quad \text{Capacitance} \equiv \frac{(As)^2}{\text{Torque/radian}}$$

Circuit Analogs of Mechanical Spring/Mass or Torque/Inertia Systems

A.

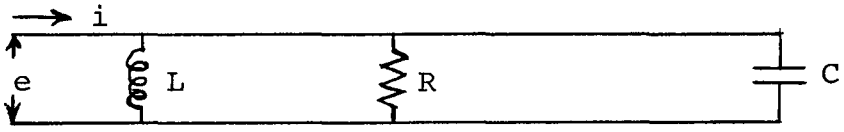


$$F = Sx + \rho \frac{dx}{dt} + M \frac{d^2x}{dt^2} \quad \text{or} \quad T = \sigma\theta + K \frac{d\theta}{dt} + J \frac{d^2\theta}{dt^2}$$

alternately

$$F = S\int \dot{x}dt + \rho\dot{x} + M \frac{d\dot{x}}{dt} \quad \text{or} \quad T = \sigma\int \dot{\theta}dt + K\dot{\theta} + J \frac{d\dot{\theta}}{dt}$$

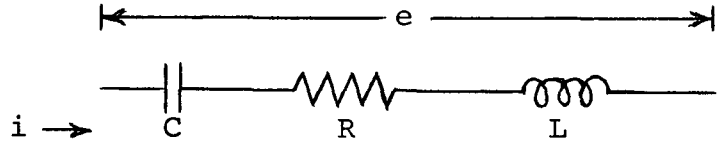
B. Magnetic Model; Velocity ≡ Voltage



$$i = \frac{1}{L}\int edt + e/R + C \frac{de}{dt}$$

equivalents F or T ≡ i, $\dot{x}$ or $\dot{\theta}$ ≡ e, S or σ ≡ $\frac{1}{L}$, ρ or K ≡ $\frac{1}{R}$,
M or J ≡ C

C. Electric Model; Force or Torque ≡ Voltage



$$e = \frac{1}{C}\int idt + iR + L \frac{di}{dt}$$

equivalents F or T ≡ e, $\dot{x}$ or $\dot{\theta}$ ≡ i, S or σ ≡ $\frac{1}{C}$, ρ or K ≡ R,
M or J ≡ L

APPENDIX G

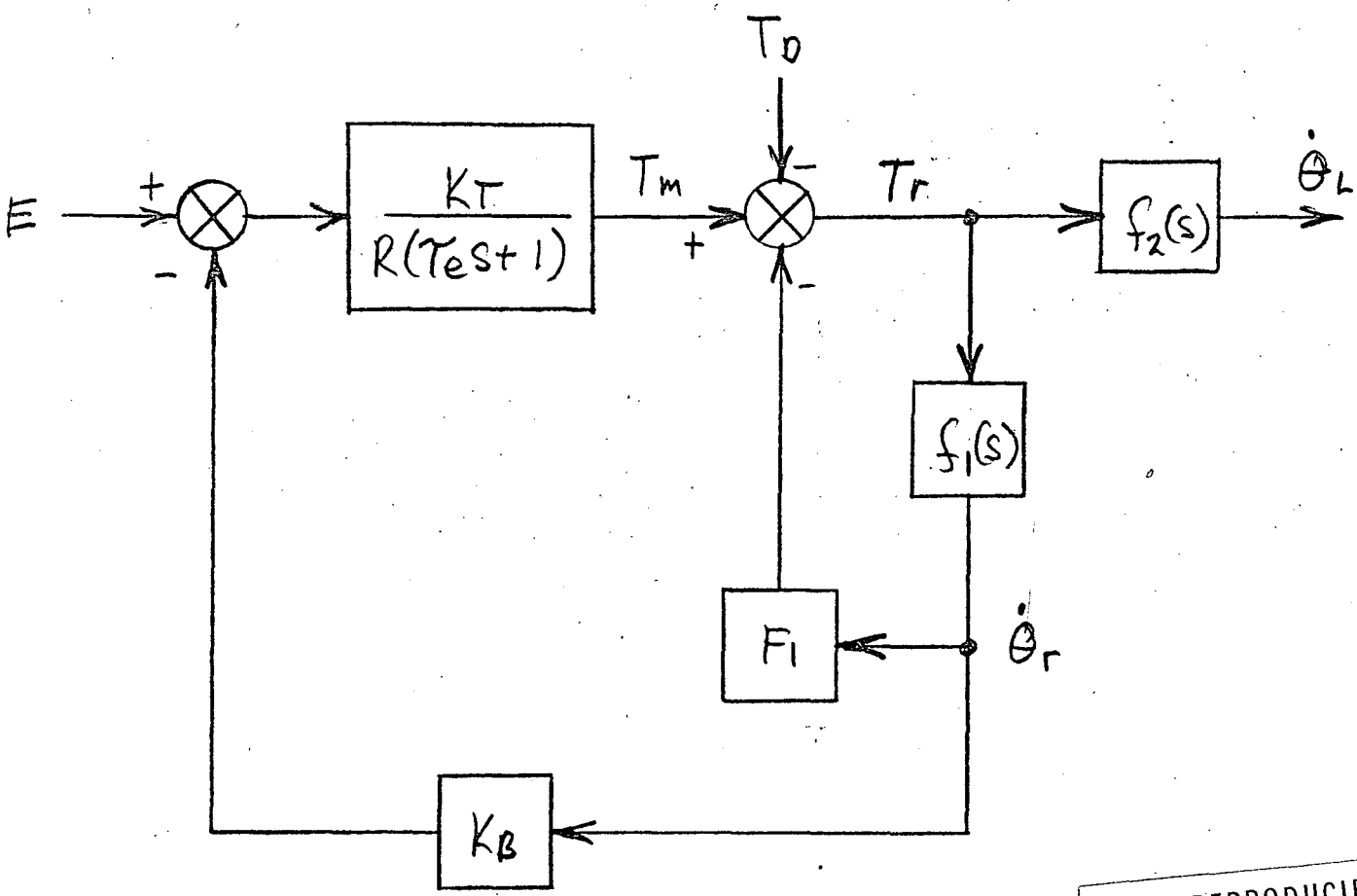
SERVO LOOP ANALYSIS, MCTR REEL-DRIVEN SYSTEM

Servo Loop Analysis

MCTR Reel Driven System

Motor Transfer Function Block Diagram

FIG. 1



Where: E = Terminal Voltage (V)
K_T = Torque Constant (N·m/A)
K_B = Motor Back EMF (V/rad/s)

Cont.
G-2

T_e = Motor Elec. Time Constant (L/R-secs)
R = Motor Winding/CKt Resistance (Ω)
T_m = Motor Torque (N·m)
T_D = Disturbance Torque (N·m)
T_r = Net Reel Torque (N·m)
F_1 = Motor Viscous Damping (N·m/rad/sec)
$f_1(s)$ = Torque-to-Reel Velocity Transfer Function
$\dot{\theta}_r$ = Reel Velocity (rad/sec)
$f_2(s)$ = Torque-to-Tape Velocity at Head Transfer Function
$\dot{\theta}_L$ = Tape Velocity at Head (rad/sec)

(all referred to idler velocity in rad/sec)

1. $T_m = \frac{K_T}{R(T_e s + 1)} (E - K_B \dot{\theta}_r)$
2. $T_r = T_m - T_D - F_1 \dot{\theta}_r$
3. $\dot{\theta}_r = f_1(s) T_r$
4. $\dot{\theta}_L = f_2(s) T_r$

3. → 1. :

5. $T_m = \frac{K_T}{R(T_e s + 1)} \cdot (E - K_B f_1(s) T_r)$

3. → 2. & solving for T_m:

6. $T_m = T_D + T_r[1 + F_1 f_1(s)]$

5. → 6.:

7. $\frac{K_T}{R(T_e s+1)}[E - K_B f_1(s) T_r] = T_D + T_r[1 + F_1 f_1(s)]$

Solving for T_r:

8. $$T_r = \frac{\frac{K_T E}{R(T_e s+1)} - T_D}{1 + \left[F_1 + \frac{K_T K_B}{R(T_e s+1)}\right] f_1(s)}$$

A new block diagram is formed as follows:

FIG. 2

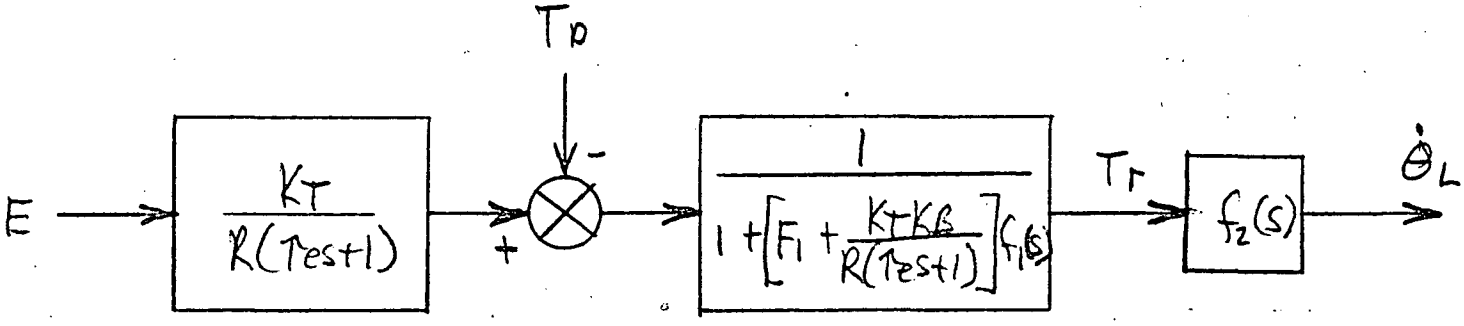
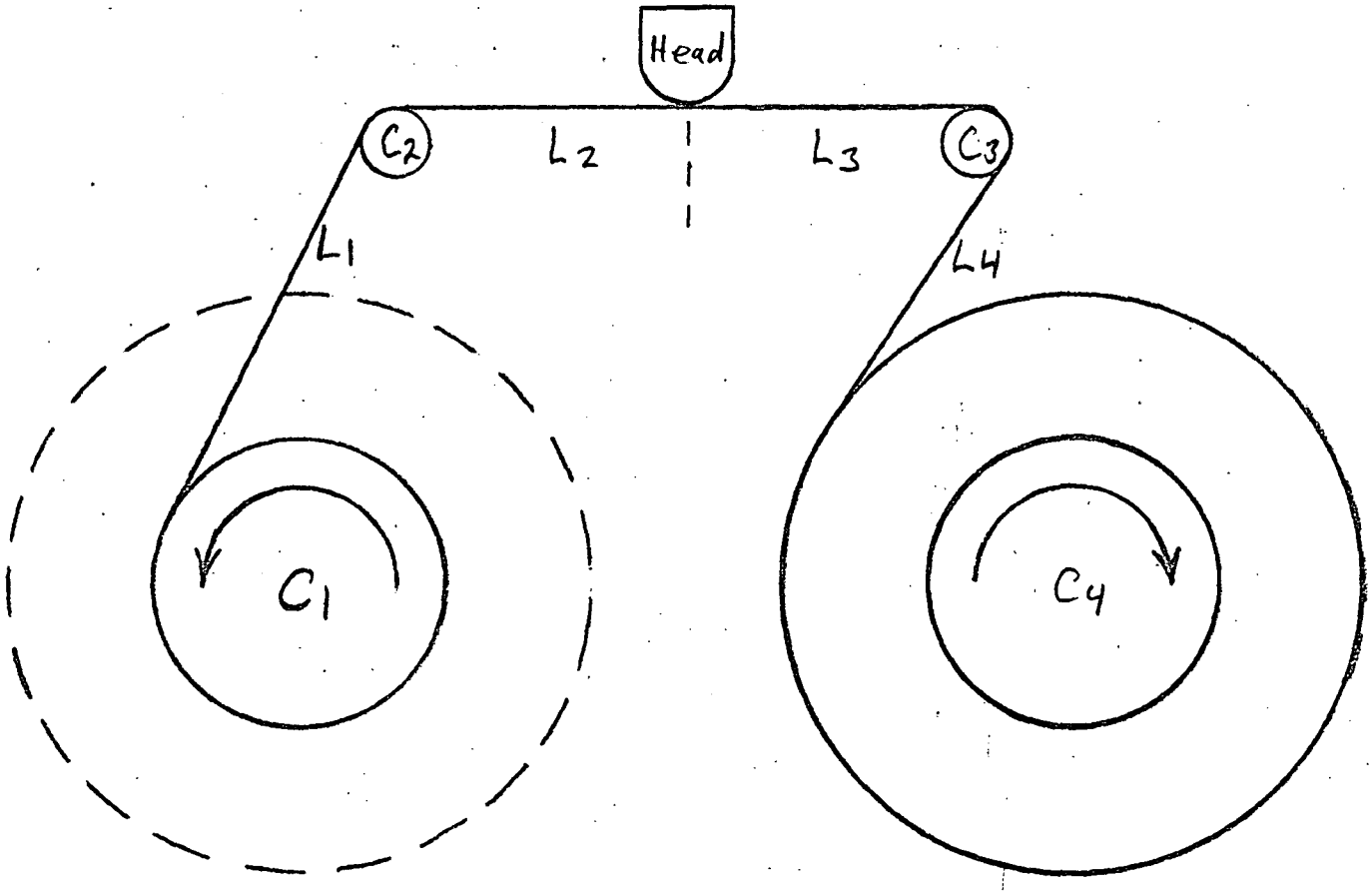
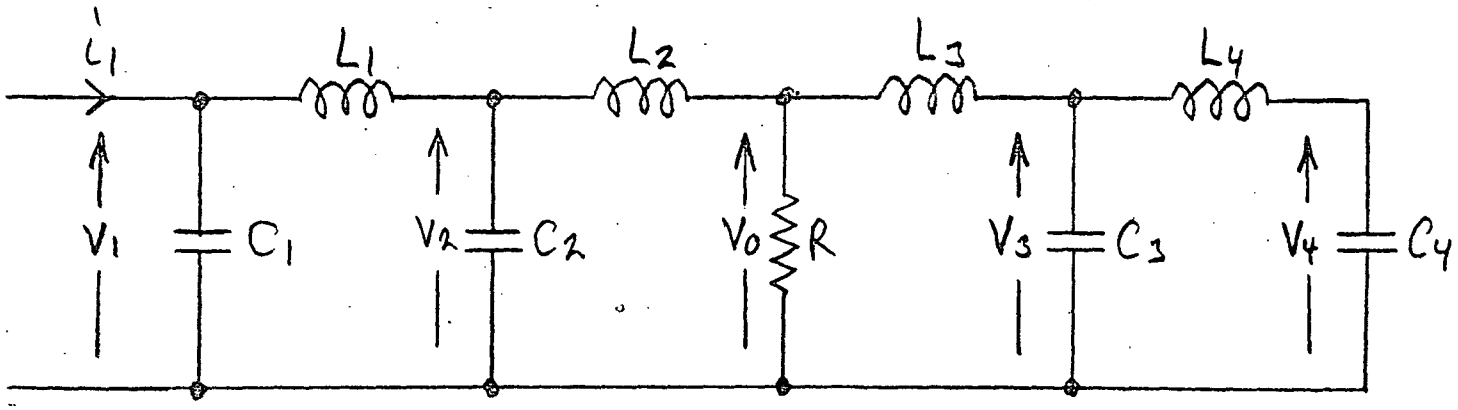


FIG. 3

MCTR Reel Drive System



Electrical Analog



The following expressions are derived for $f_1(s)$ & $f_2(s)$:

$$f_1(s) = \frac{V_1}{i_1} = R \left[\begin{array}{l} 1 + \frac{(L_1+L_2)}{R} s + (L_2+L_4) C_4 s^2 \\ + \frac{(L_1L_2 + L_1L_4 + L_2L_4 + L_2^2) C_4 s^3}{R} \\ + (L_1L_4 + L_2L_4 + L_1L_2) C_2 C_4 s^4 \\ + \frac{(2L_1L_2L_4 + L_1L_2^2 + L_2^2L_4) C_2 C_4 s^5}{R} \\ + L_1L_2L_4 C_2^2 C_4 s^6 + \frac{L_1L_2^2L_4 C_2^2 C_4 s^7}{R} \end{array} \right]$$

$$\left\{ \begin{array}{l} 1 + C_1Rs + [C_1(L_1+L_2) + C_4(L_2+L_4)] s^2 \\ + (L_2+L_4) C_1 C_4 R s^3 + (L_1L_4 + L_1L_2 + L_2L_4 + L_2^2) C_1 C_4 s^4 \\ + (L_1L_2 + L_1L_4 + L_2L_4) C_1 C_2 C_4 R s^5 \\ + (2L_1L_2L_4 + L_1L_2^2 + L_2^2L_4) C_1 C_2 C_4 s^6 \\ + L_1L_2L_4 C_1 C_2^2 C_4 R s^7 + L_1L_2^2L_4 C_1 C_2^2 C_4 s^8 \end{array} \right\}$$

$$f_2(S) = \frac{V_o}{V_i} = \frac{\left[1 + (L_2+L_4)C_4S^2 + L_2L_4C_2C_4S^4\right]}{\left\{\begin{array}{l} 1 + C_1RS + \left[C_1(L_1+L_2) + C_4(L_2+L_4)\right]S^2 \\ +(L_2+L_4)C_1C_4RS^3 + (L_1L_4 + L_1L_2 + L_2L_4 + L_2^2)C_1C_4S^4 \\ +(L_1L_2 + L_1L_4 + L_2L_4)C_1C_2C_4RS^5 \\ +(2L_1L_2L_4 + L_1L_2^2 + L_2^2L_4)C_1C_2C_4S^6 \\ +L_1L_2L_4C_1C_2^2C_4RS^7 + L_1L_2^2L_4C_1C_2^2C_4S^8 \end{array}\right\}}$$

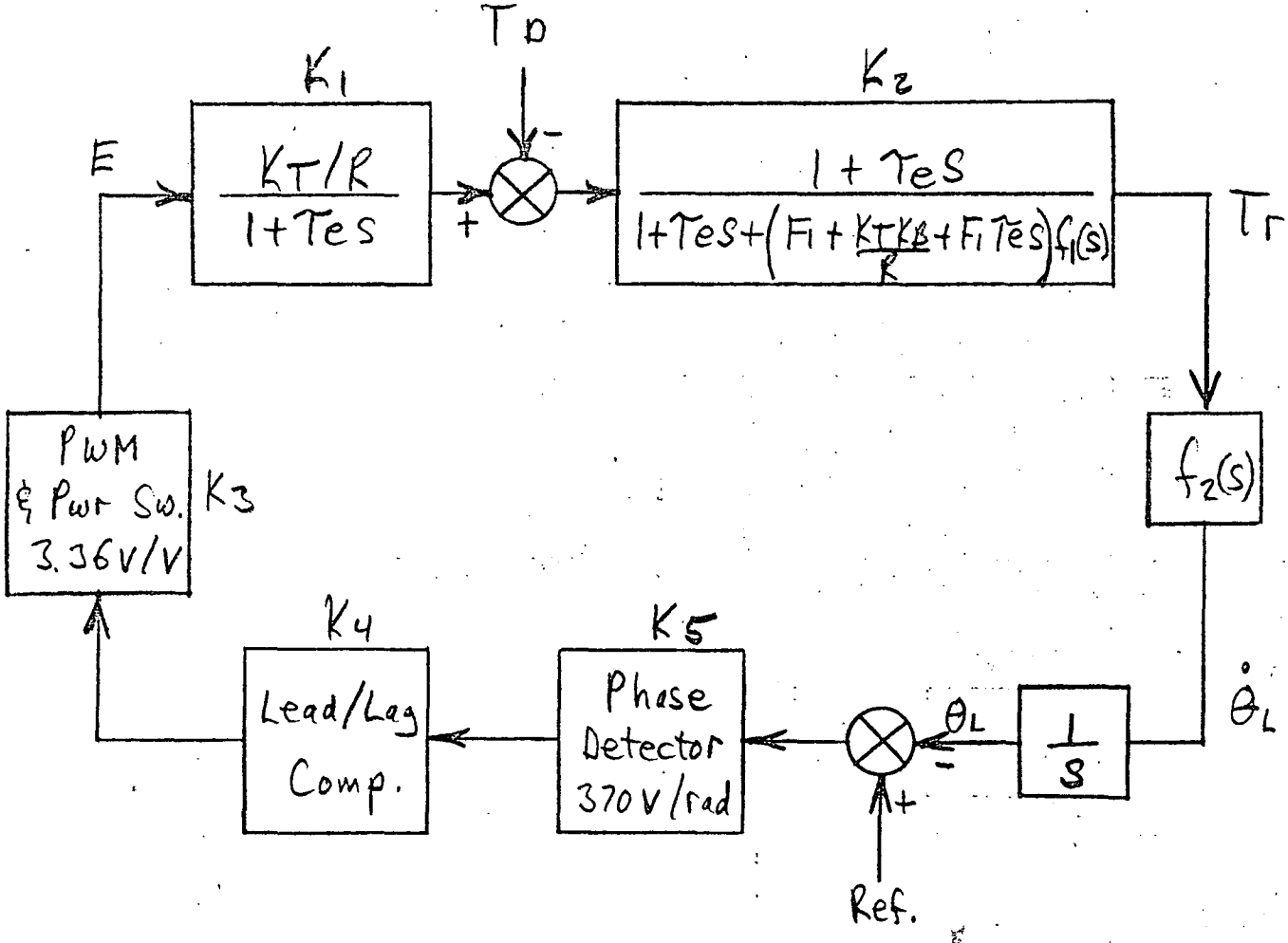
Assuming that:

$$C_2 = C_3$$
$$C_1 >> C_2$$
$$C_4 >> C_2$$
$$L_2 = L_3$$

Where:		Start-of-Tape	Mid-Tape	End-of-Tape
R	=	$187 \cdot 10^3 \Omega$	$187 \cdot 10^3 \Omega$	$187 \cdot 10^3 \Omega$
C_1	=	76.8 μf	140 μf	207 μf
(Idler Dia.: 1/2" / 1") C_2	=	.88/3.37 μf	.88/3.37 μf	.88/3.37 μf
C_4	=	207 μf	140 μf	76.8 μf
L_1	=	126.7 mh	110.3 mh	63.4 mh
L_2	=	63.4 mh	63.4 mh	63.4 mh
L_4	=	63.4 mh	110.3 mh	126.7 mh

FIG. 4

Complete MCTR Reel Drive Servo Loop



$$f_1(s) = \frac{\dot{\theta}_r}{T_r} = \frac{V_1}{i_1}$$

$$f_2(s) = \frac{\dot{\theta}_L}{T_r} = \frac{V_0}{i_1}$$

Open-Loop Gain:

$$G = K_1 \cdot K_2 \cdot K_3 \cdot K_4 \cdot K_5 \cdot \frac{1}{s} \cdot f_2(s)$$

Flutter (Due to Torque Disturbance):

$$\frac{\dot{\theta}_L}{T_D} = \frac{-K_2 \cdot f_2(s)}{1 - \frac{K_2 \cdot f_2(s) \cdot K_1 \cdot K_3 \cdot K_4 \cdot K_5}{s}}$$

Jitter (Due to Torque Disturbance):

$$\frac{\theta_L}{T_D} = \frac{\dot{\theta}_L}{T_D} \cdot s$$